Chapter 6. Converter Circuits

6.1. Circuit manipulations

6.2. A short list of converters

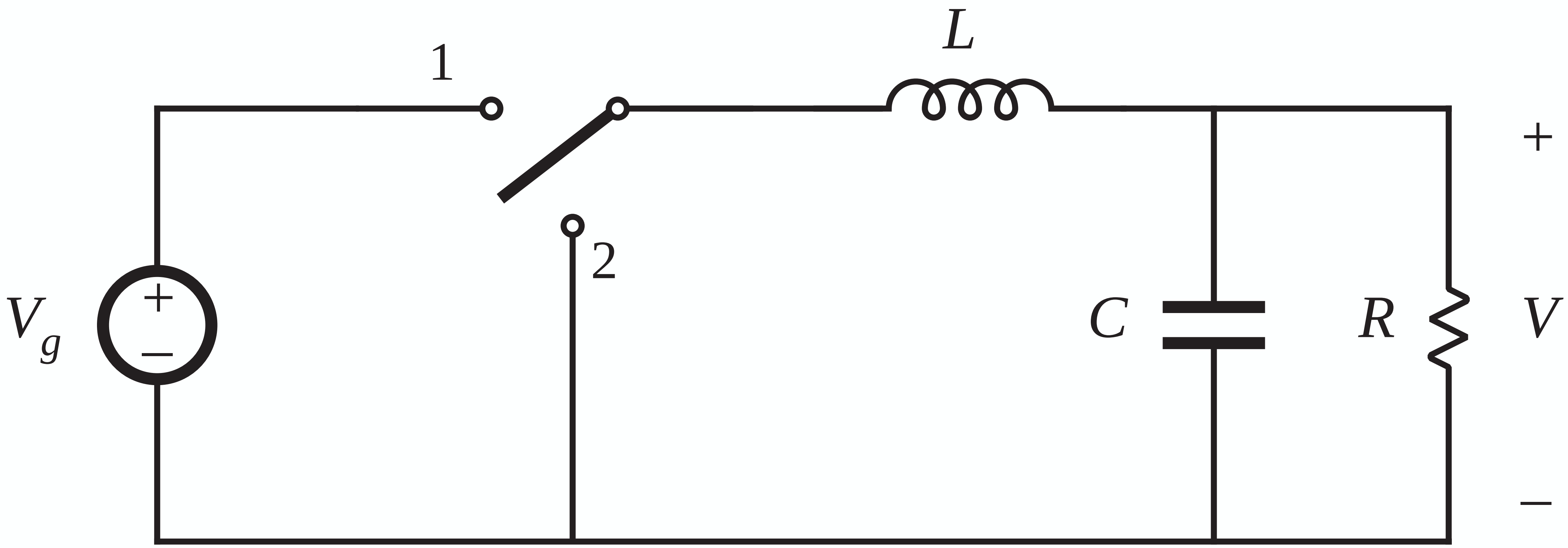
6.3. Transformer isolation

6.4. Converter evaluation and design

6.5. Summary of key points

- Where do the boost, buck-boost, and other converters originate?
- How can we obtain a converter having given desired properties?
- What converters are possible?
- How can we obtain transformer isolation in a converter?
- For a given application, which converter is best?

6.1. Circuit Manipulations



Begin with buck converter: derived in Chapter 1 from first principles

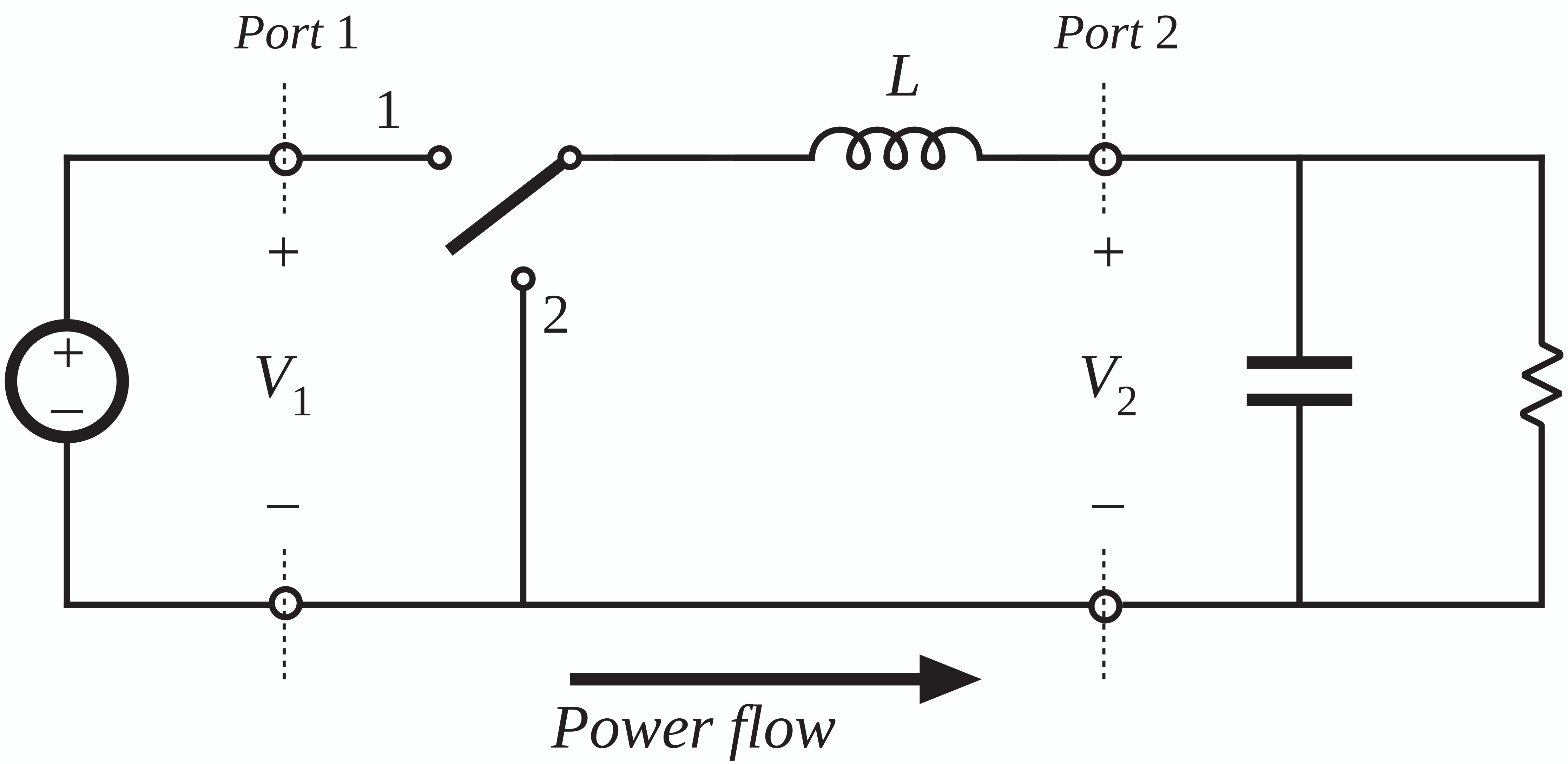
- Switch changes dc component, low-pass filter removes switching harmonics
- Conversion ratio is $M = D$

6.1.1. Inversion of source and load

Interchange power input and output ports of a converter

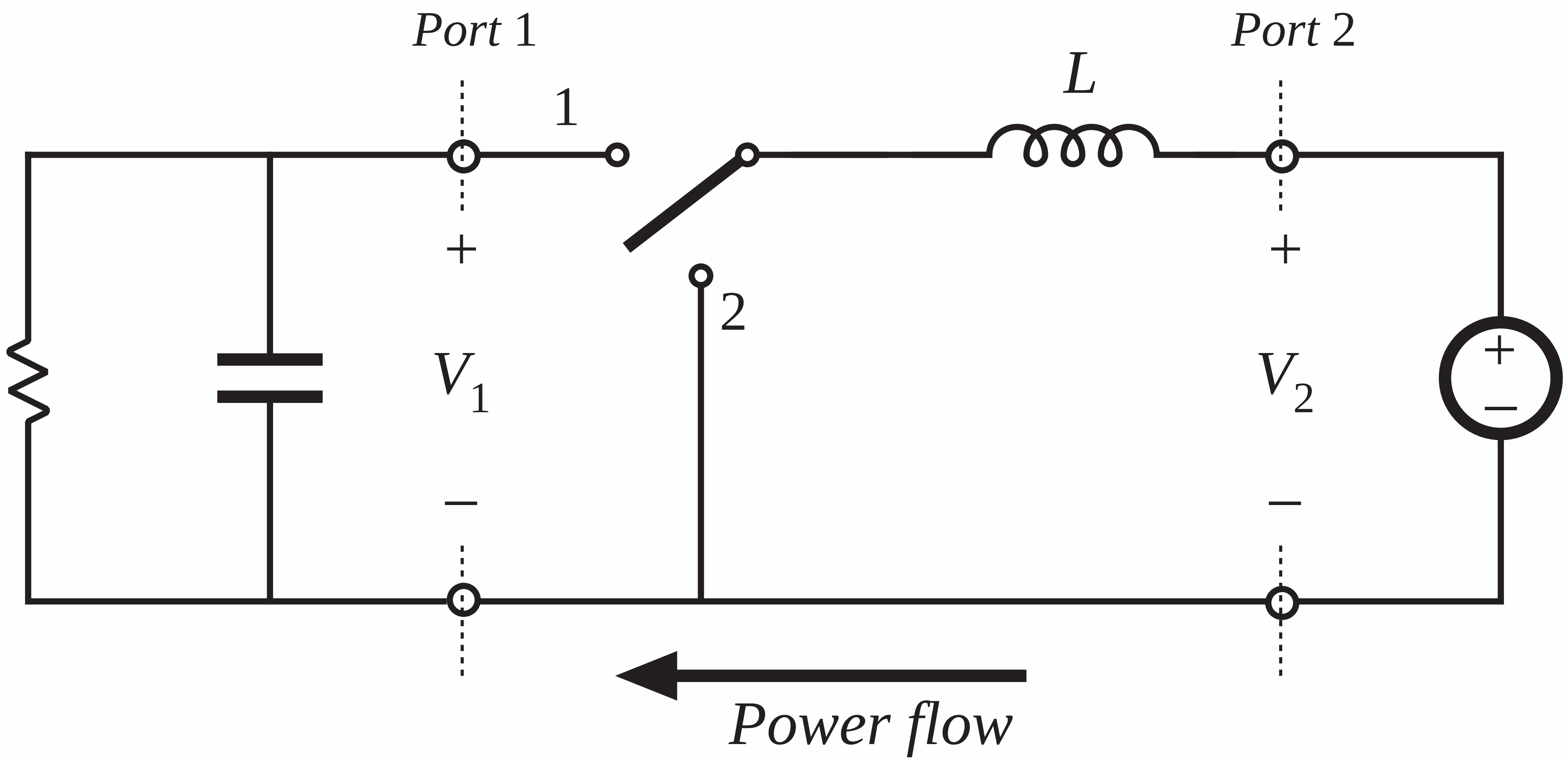
Buck converter example

$$V_2 = DV_1$$



Inversion of source and load

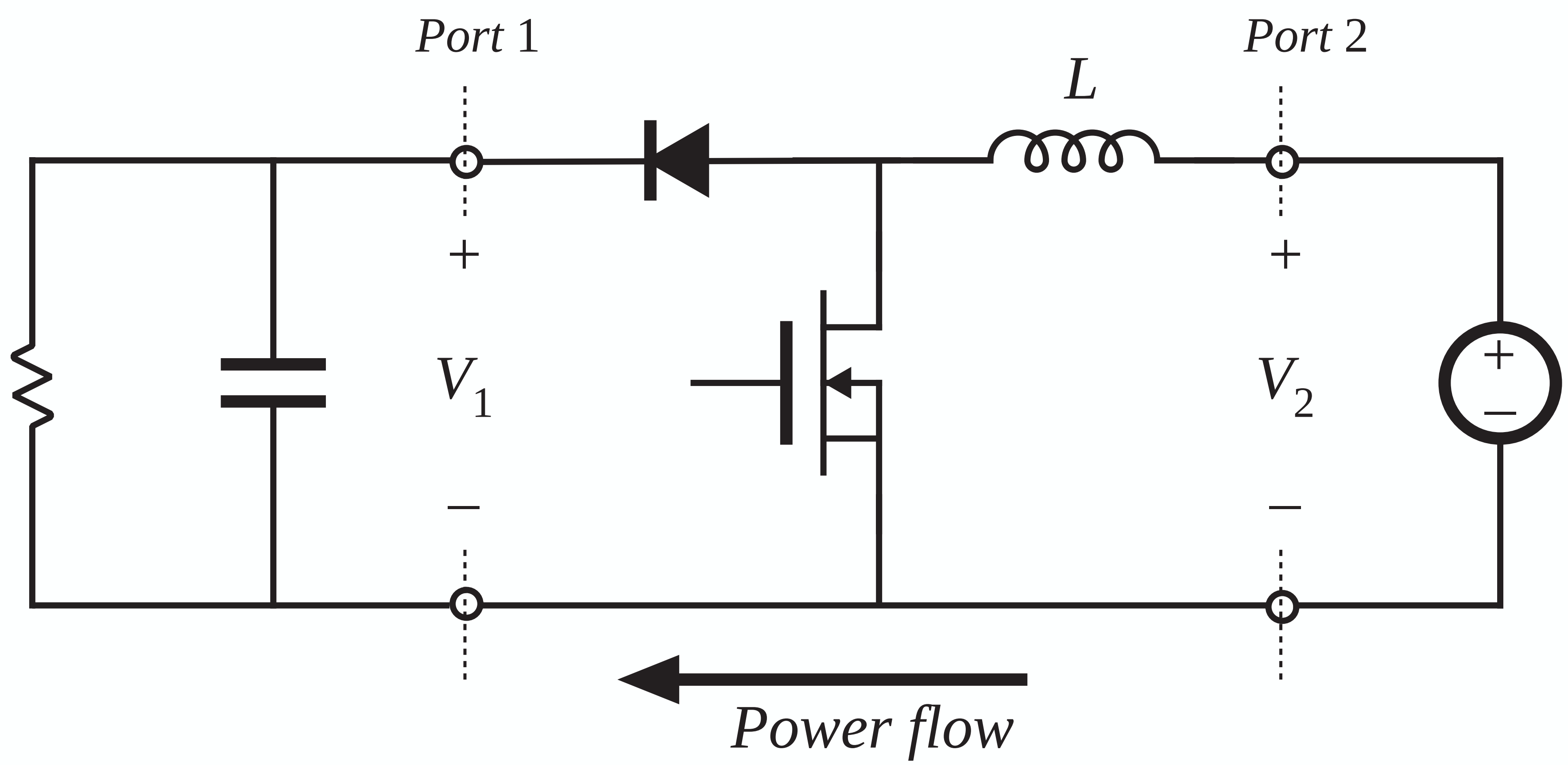
Interchange power source and load:



$$V_2 = DV_1 \qquad V_1 = \frac{1}{D} V_2$$

Realization of switches as in Chapter 4

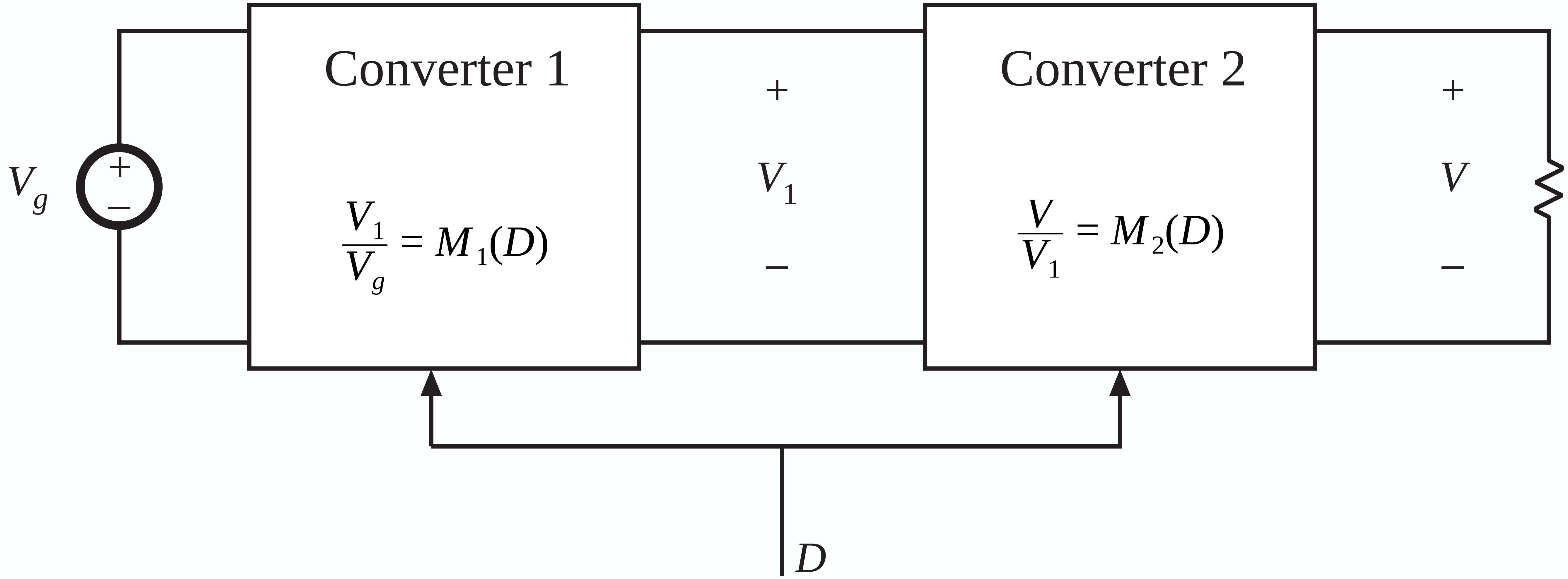
- Reversal of power flow requires new realization of switches
- Transistor conducts when switch is in position 2
- Interchange of D and D'



$$V_1 = \frac{1}{D'} V_2$$

Inversion of buck converter yields boost converter

6.1.2. Cascade connection of converters

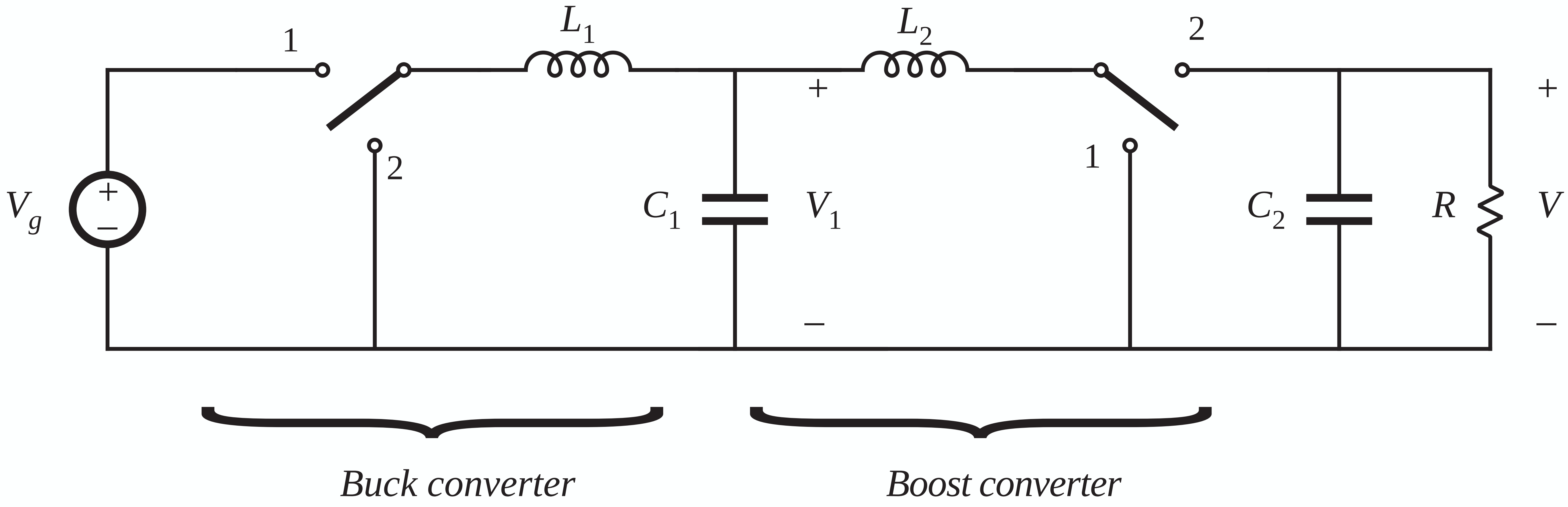


$$V_1 = M_1(D)V_g$$

$$V = M_2(D)V_1$$

$$\frac{V}{V_g} = M(D) = M_1(D)M_2(D)$$

Example: buck cascaded by boost



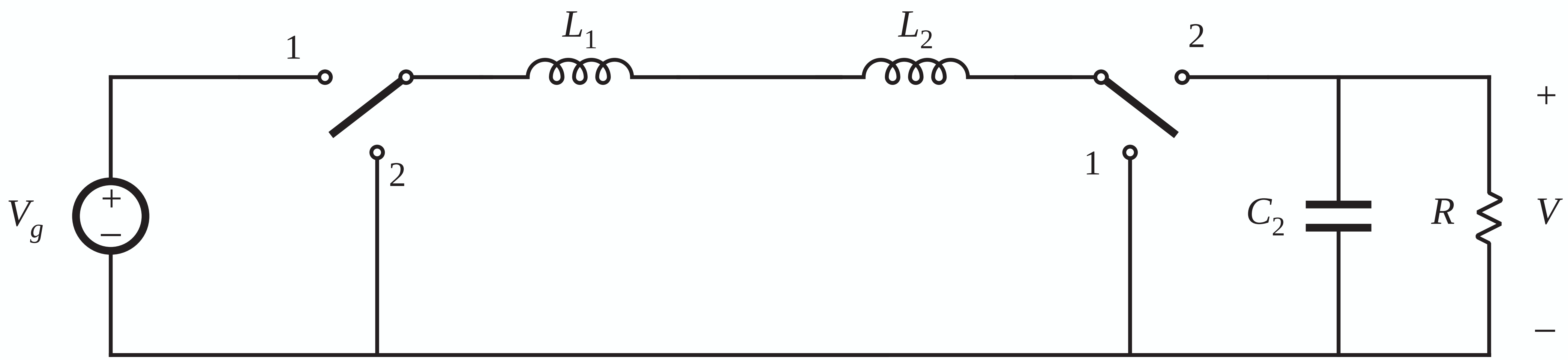
$$\frac{V_1}{V_g} = D$$

$$\frac{V}{V_1} = \frac{1}{1-D}$$

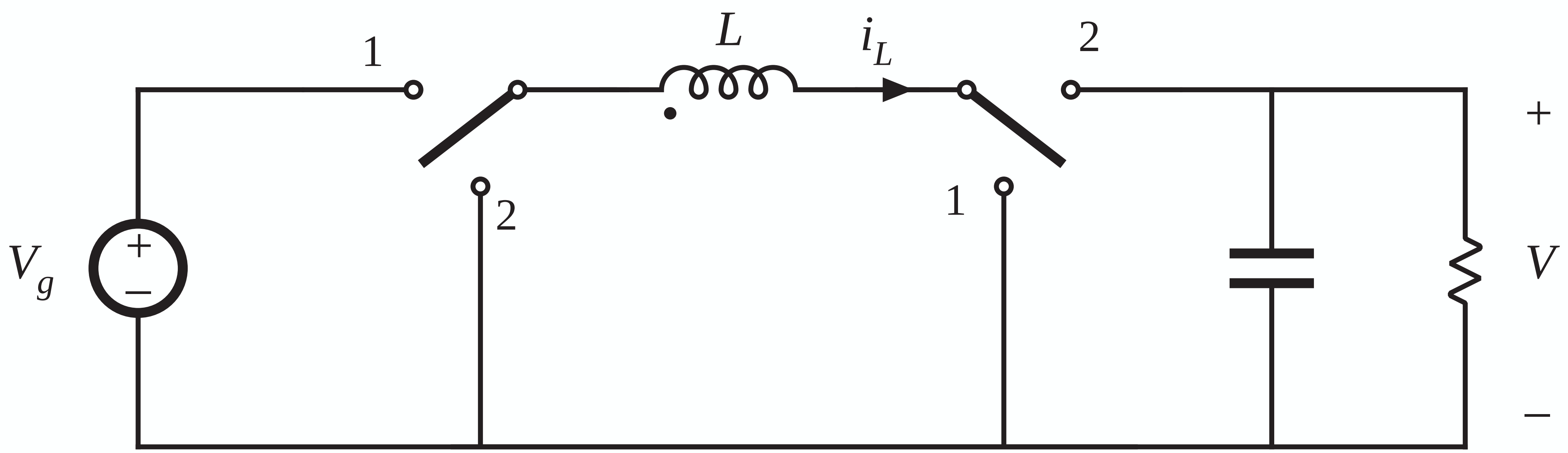
$$\longrightarrow \quad \frac{V}{V_g} = \frac{D}{1-D}$$

Buck cascaded by boost: simplification of internal filter

Remove capacitor C_1

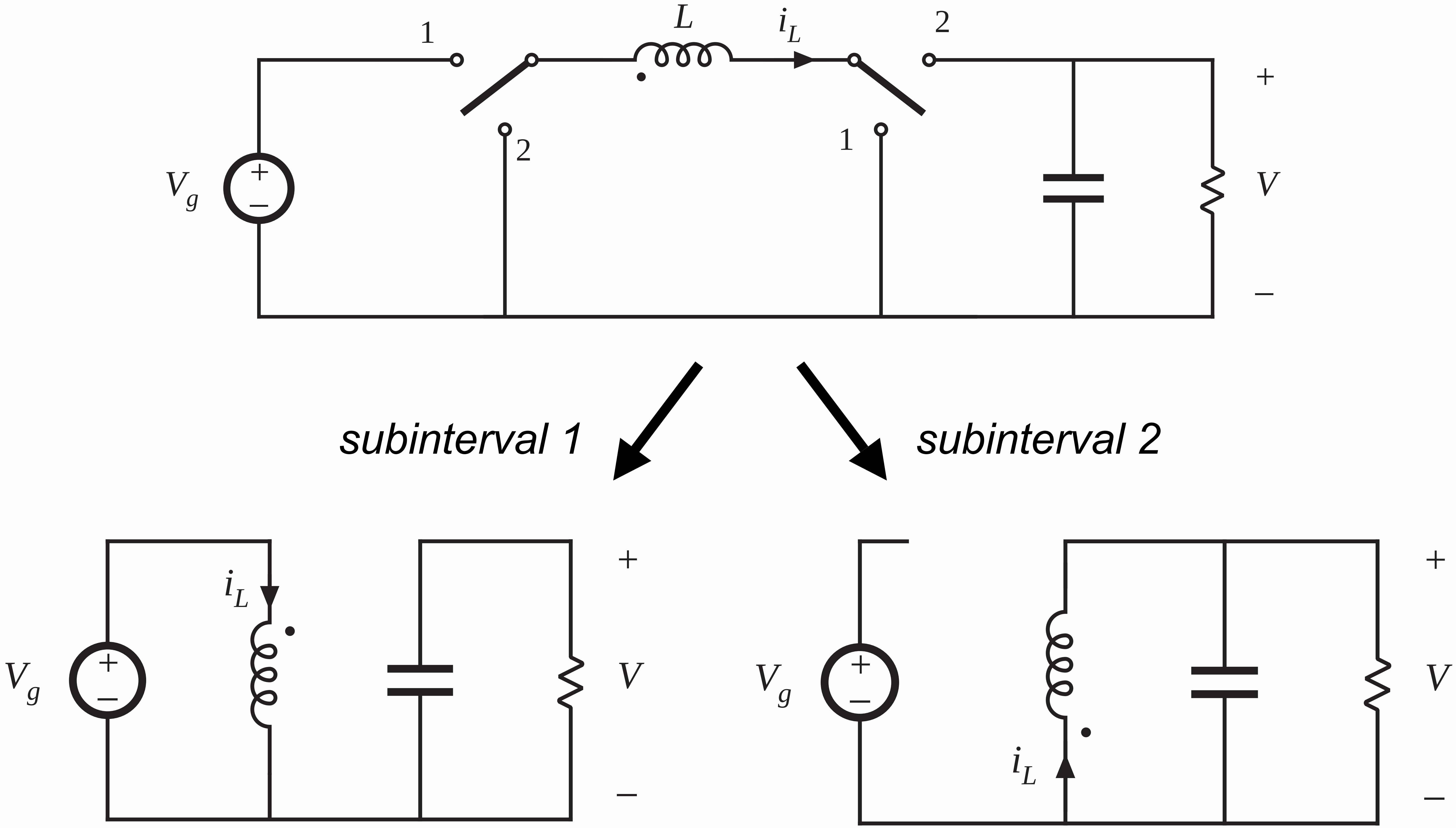


Combine inductors L_1 and L_2



Noninverting buck-boost converter

Noninverting buck-boost converter

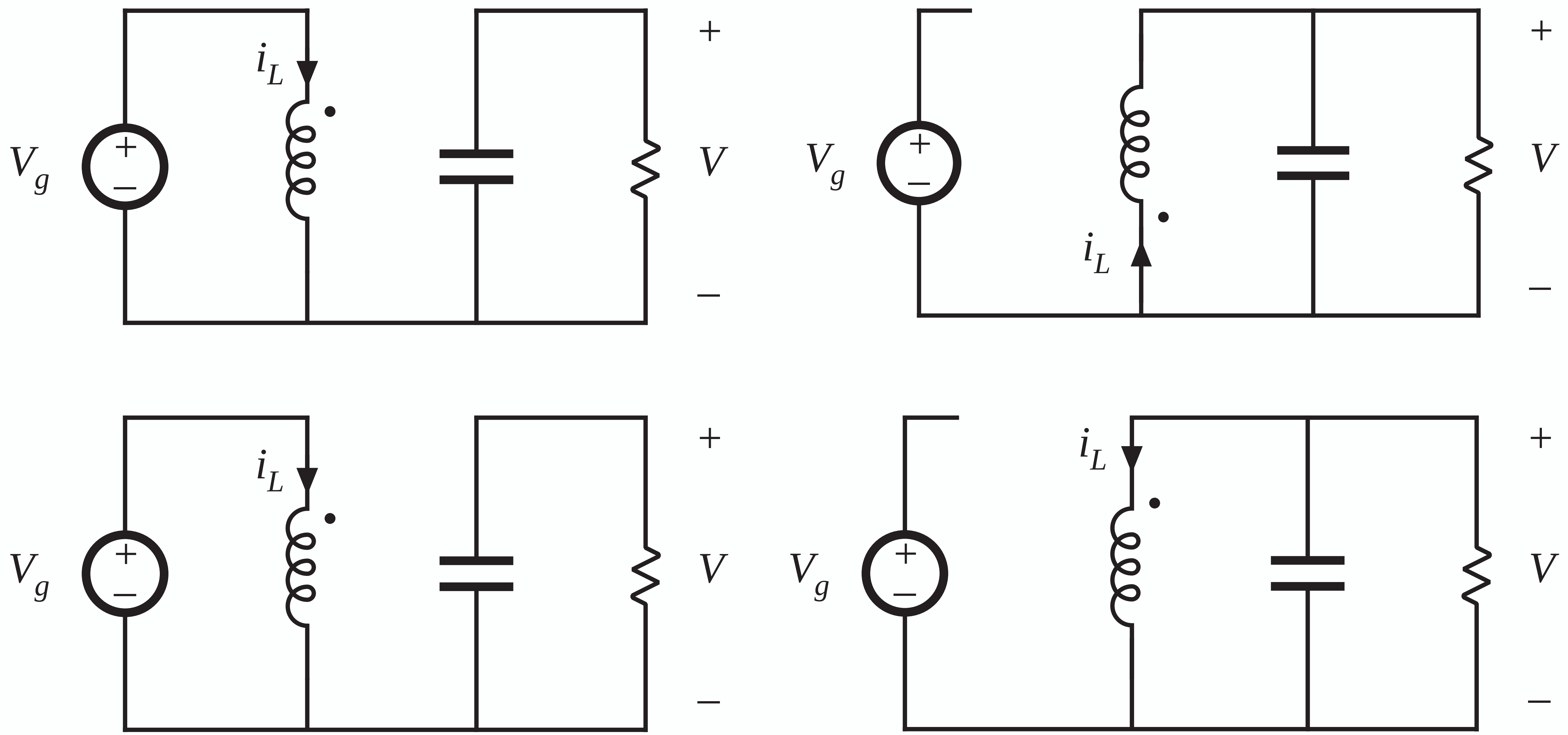


Reversal of output voltage polarity

subinterval 1 *subinterval 2*

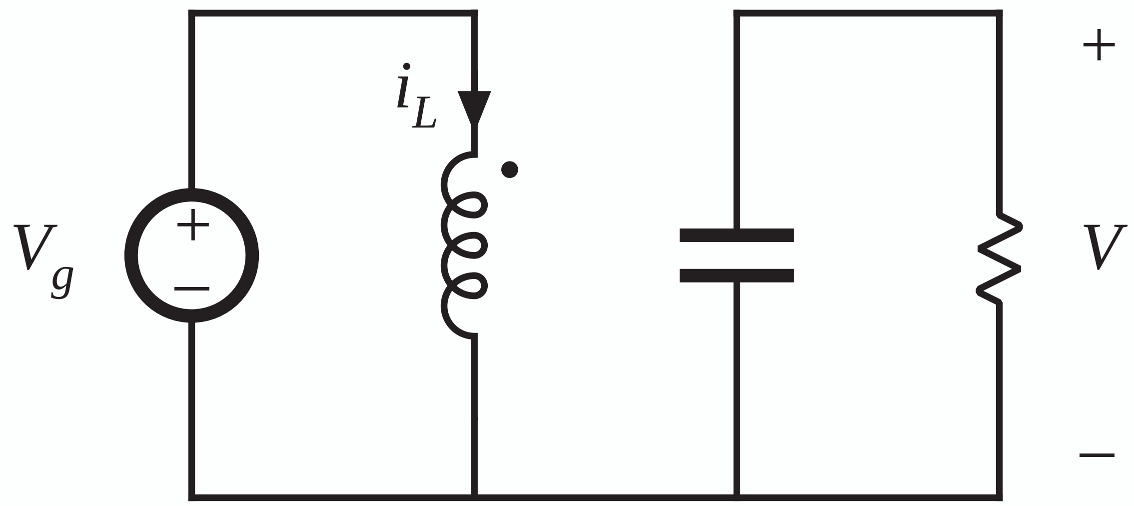
noninverting buck-boost

inverting buck-boost

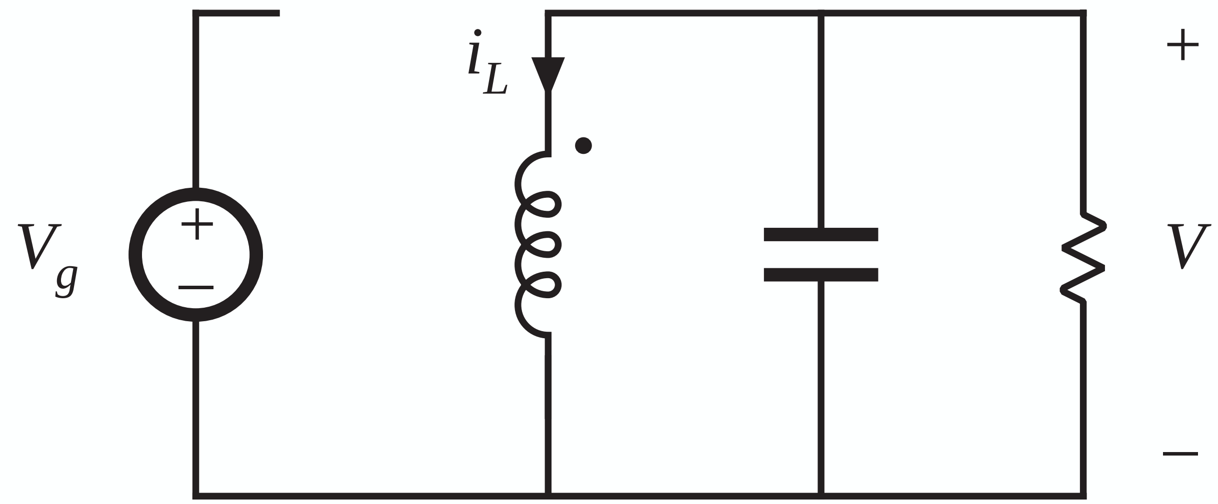


Reduction of number of switches: inverting buck-boost

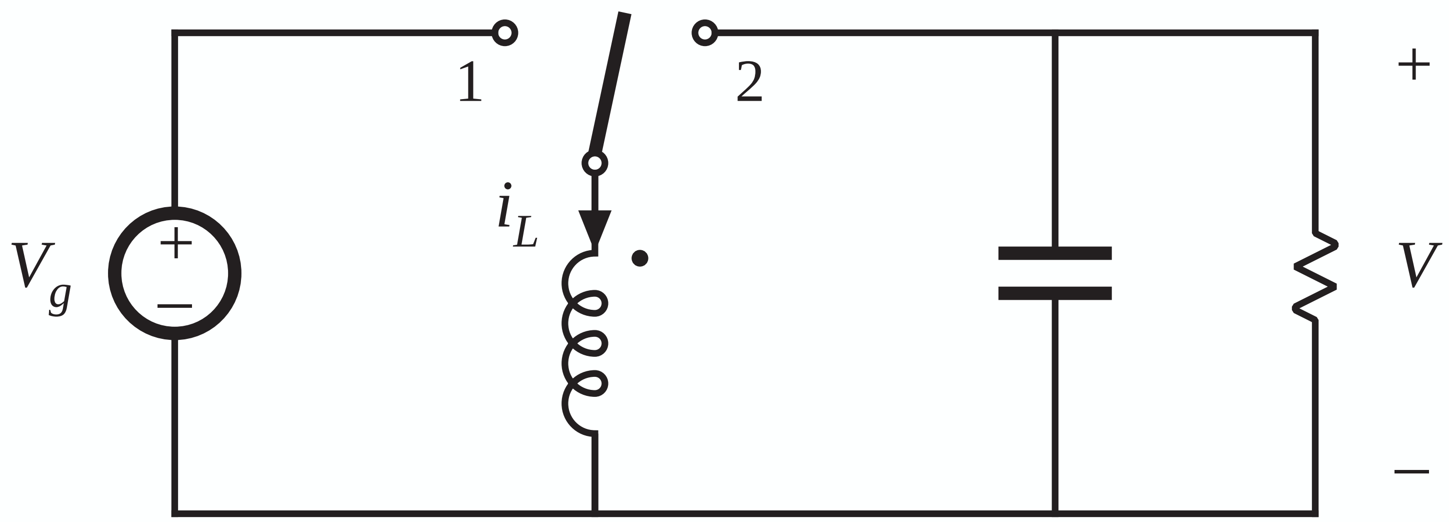
Subinterval 1



Subinterval 2



One side of inductor always connected to ground
— hence, only one SPDT switch needed:



$$\frac{V}{V_g} = -\frac{D}{1-D}$$

Discussion: cascade connections

- Properties of buck-boost converter follow from its derivation as buck cascaded by boost

  Equivalent circuit model: buck 1:D transformer cascaded by boost D':1 transformer

  Pulsating input current of buck converter

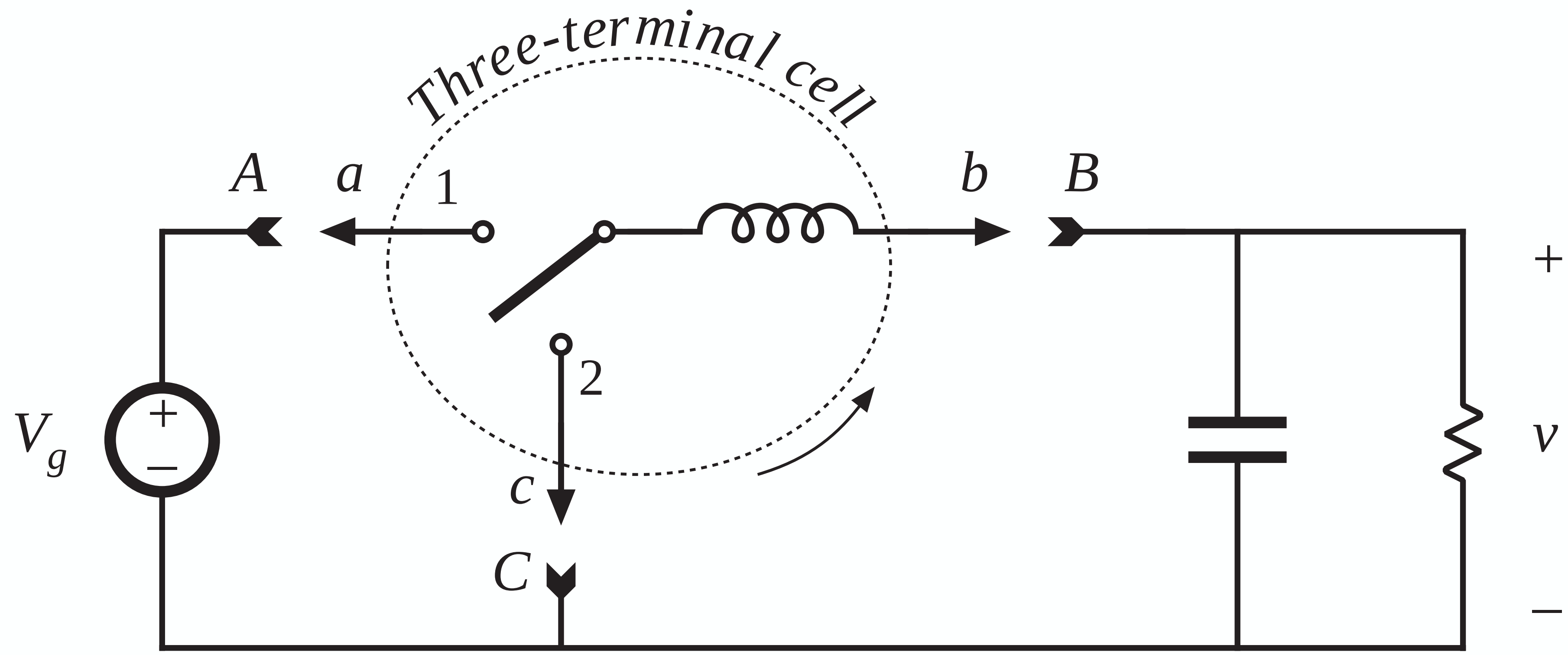
  Pulsating output current of boost converter

- Other cascade connections are possible

  Cuk converter: boost cascaded by buck

6.1.3. Rotation of three-terminal cell

Treat inductor and SPDT switch as three-terminal cell:

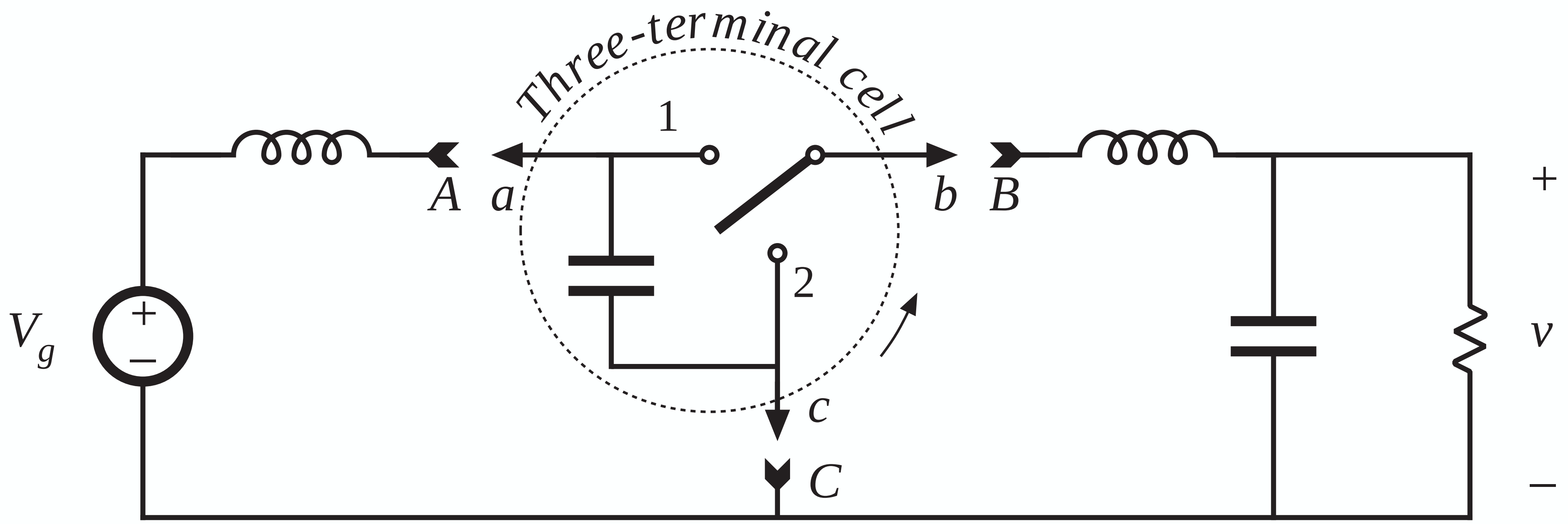


Three-terminal cell can be connected between source and load in three nontrivial distinct ways:

a-A b-B c-C	buck converter
a-C b-A c-B	boost converter
a-A b-C c-B	buck-boost converter

Rotation of a dual three-terminal network

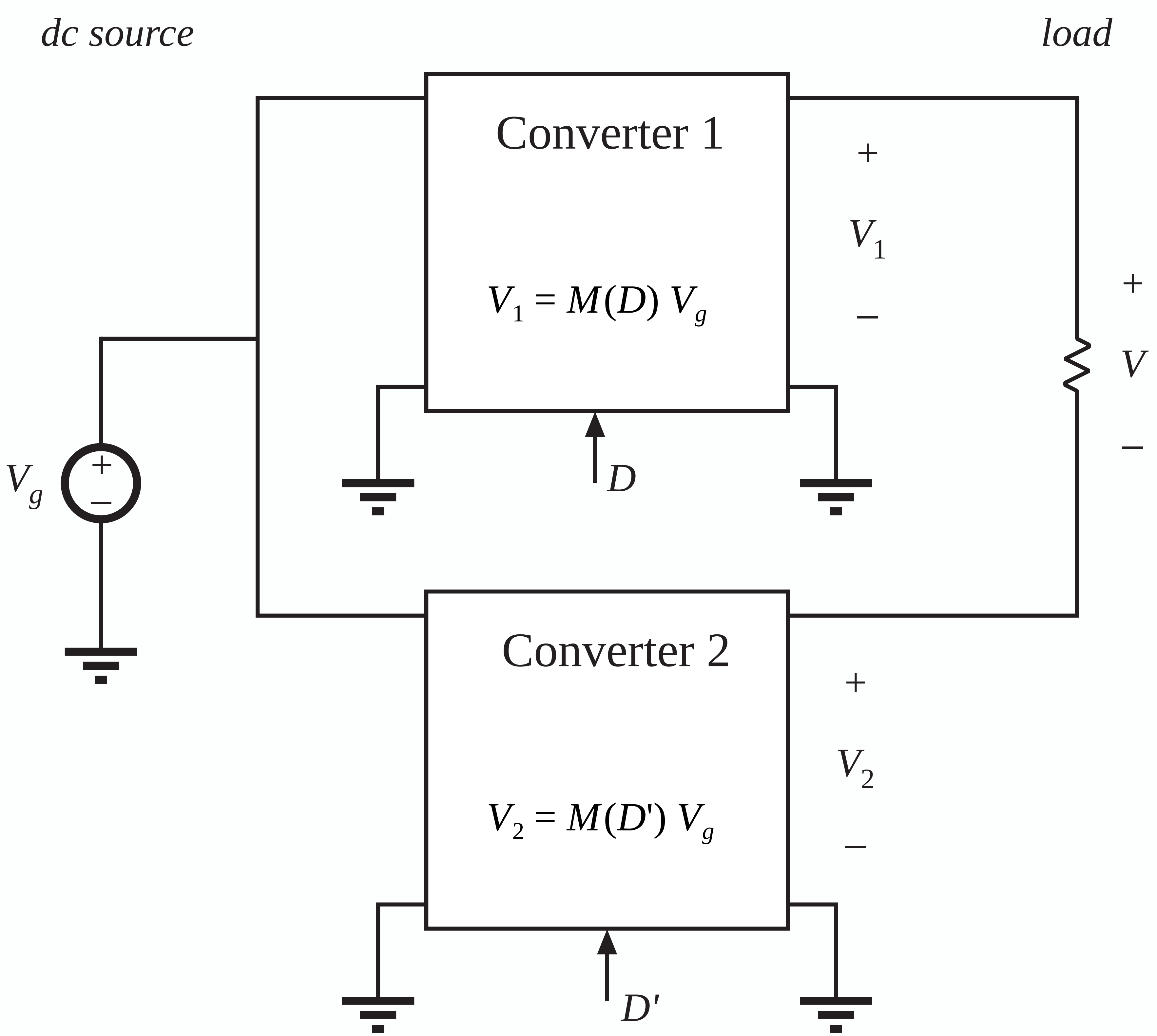
A capacitor and SPDT switch as a three-terminal cell:



Three-terminal cell can be connected between source and load in three nontrivial distinct ways:

a-A b-B c-C	buck converter with L-C input filter
a-C b-A c-B	boost converter with L-C output filter
a-A b-C c-B	Cuk converter

6.1.4. Differential connection of load to obtain bipolar output voltage

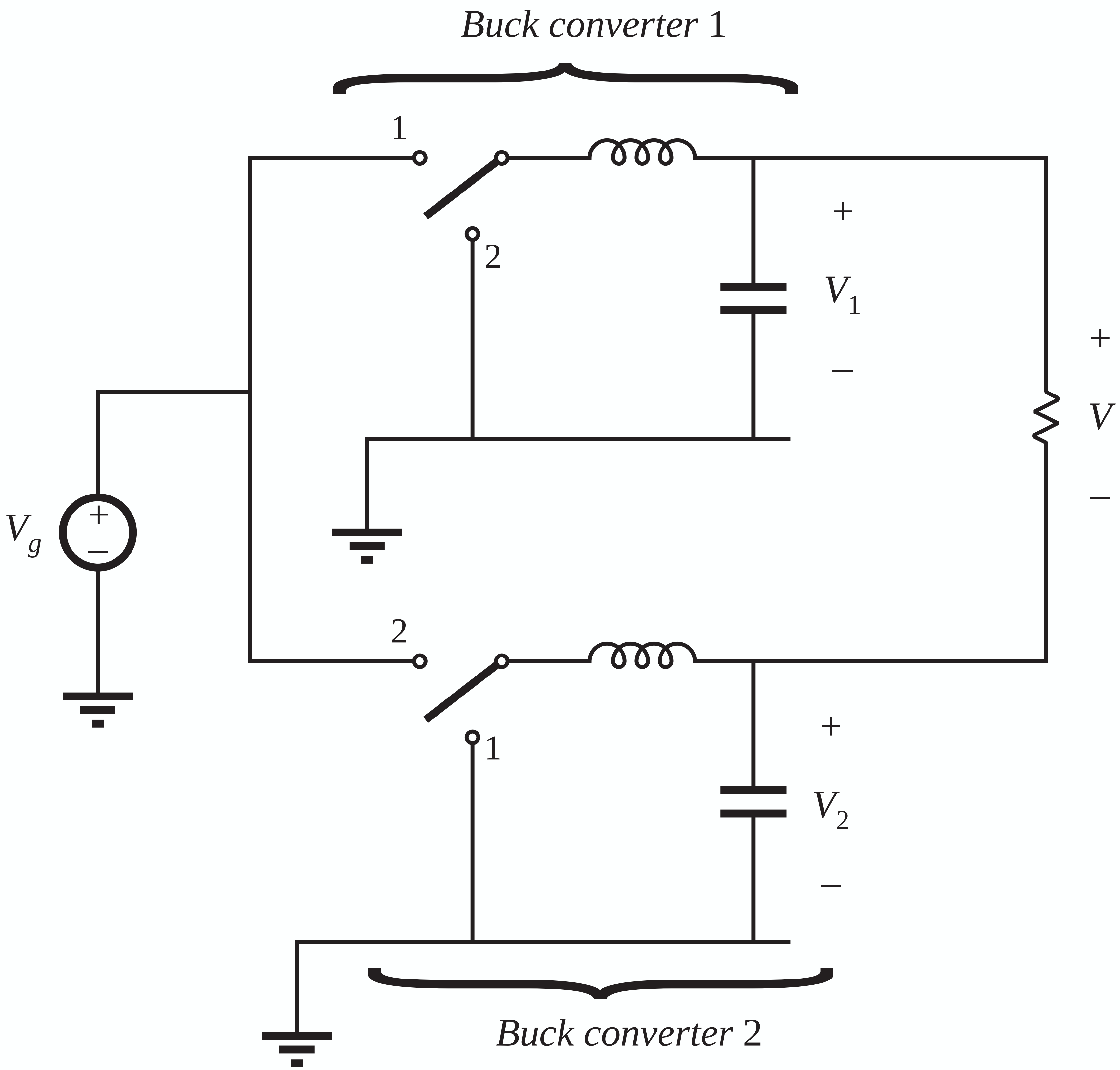


Differential load voltage is

$$V = V_1 - V_2$$

The outputs V_1 and V_2 may both be positive, but the differential output voltage V can be positive or negative.

Differential connection using two buck converters



Converter #1 transistor driven with duty cycle D

Converter #2 transistor driven with duty cycle complement D'

Differential load voltage is

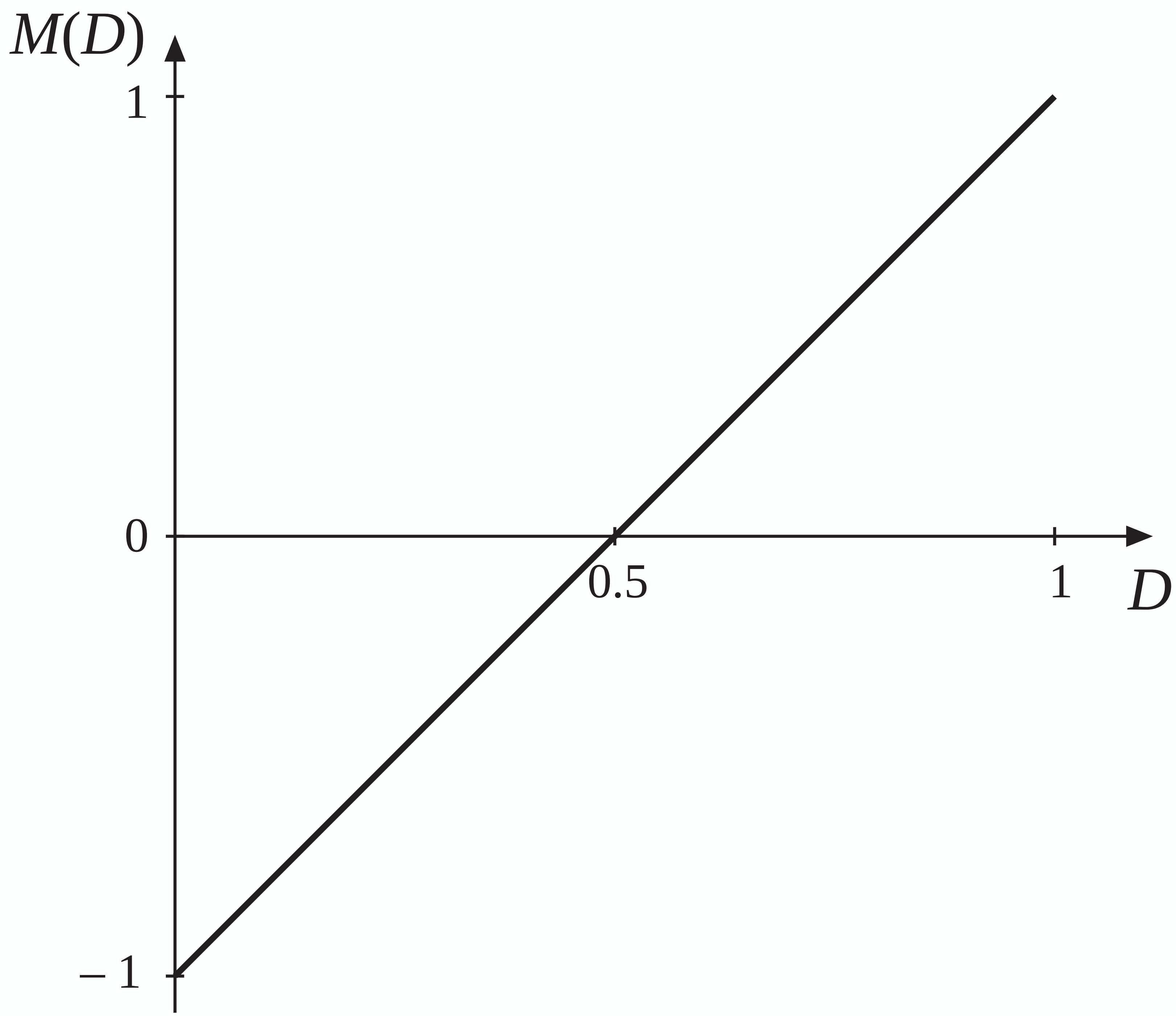
$$V = DV_g - D'V_g$$

Simplify:

$$V = (2D - 1)V_g$$

Conversion ratio $M(D)$, differentially-connected buck converters

$$V = (2D - 1)V_g$$



6.2. A short list of converters

An infinite number of converters are possible, which contain switches embedded in a network of inductors and capacitors

Two simple classes of converters are listed here:

- Single-input single-output converters containing a single inductor. The switching period is divided into two subintervals. This class contains eight converters.
- Single-input single-output converters containing two inductors. The switching period is divided into two subintervals. Several of the more interesting members of this class are listed.

Single-input single-output converters containing one inductor

- Use switches to connect inductor between source and load, in one manner during first subinterval and in another during second subinterval
- There are a limited number of ways to do this, so all possible combinations can be found
- After elimination of degenerate and redundant cases, eight converters are found:

dc-dc converters

buck boost buck-boost noninverting buck-boost

dc-ac converters

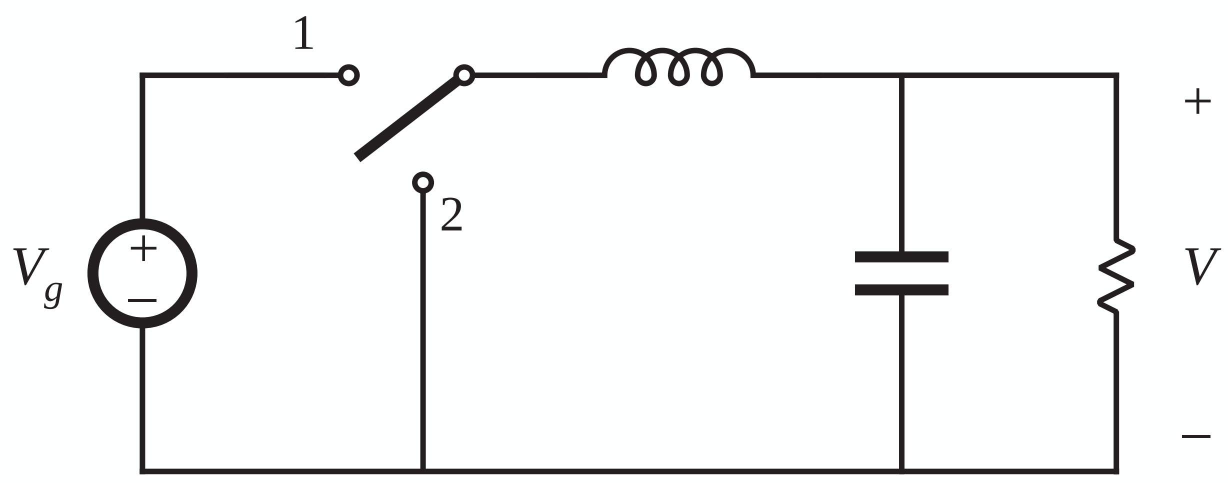
bridge Watkins-Johnson

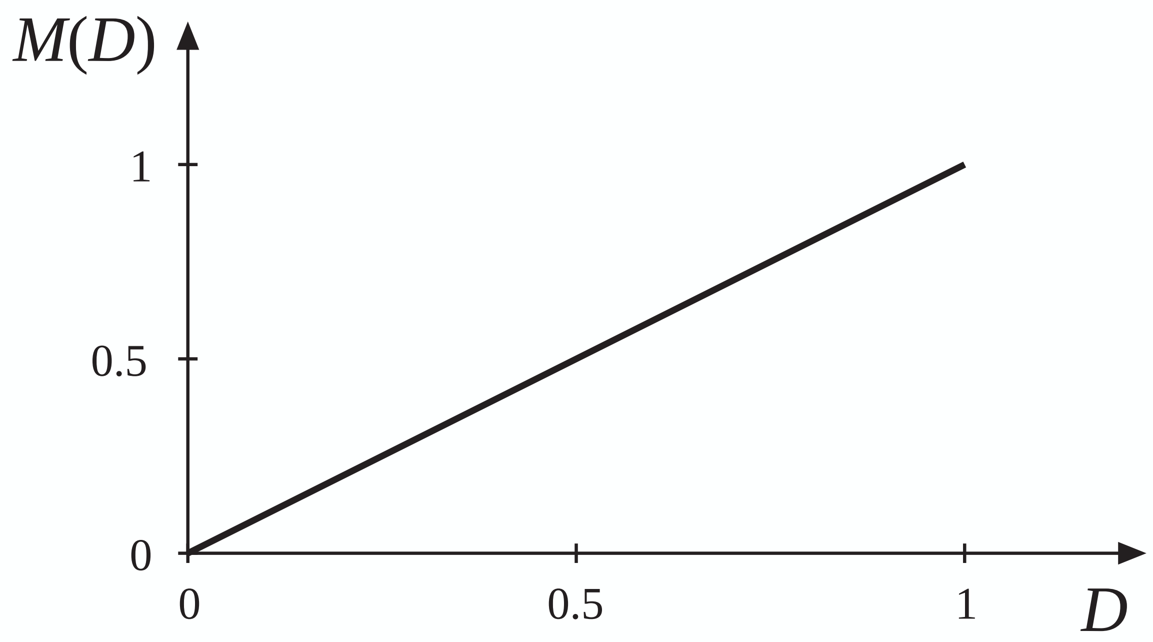
ac-dc converters

current-fed bridge inverse of Watkins-Johnson

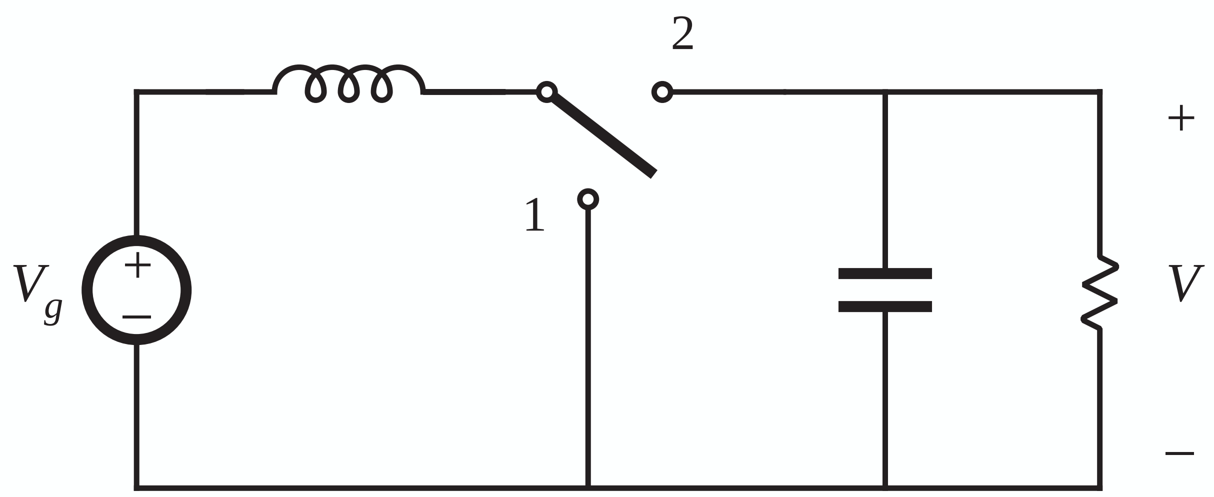
Converters producing a unipolar output voltage

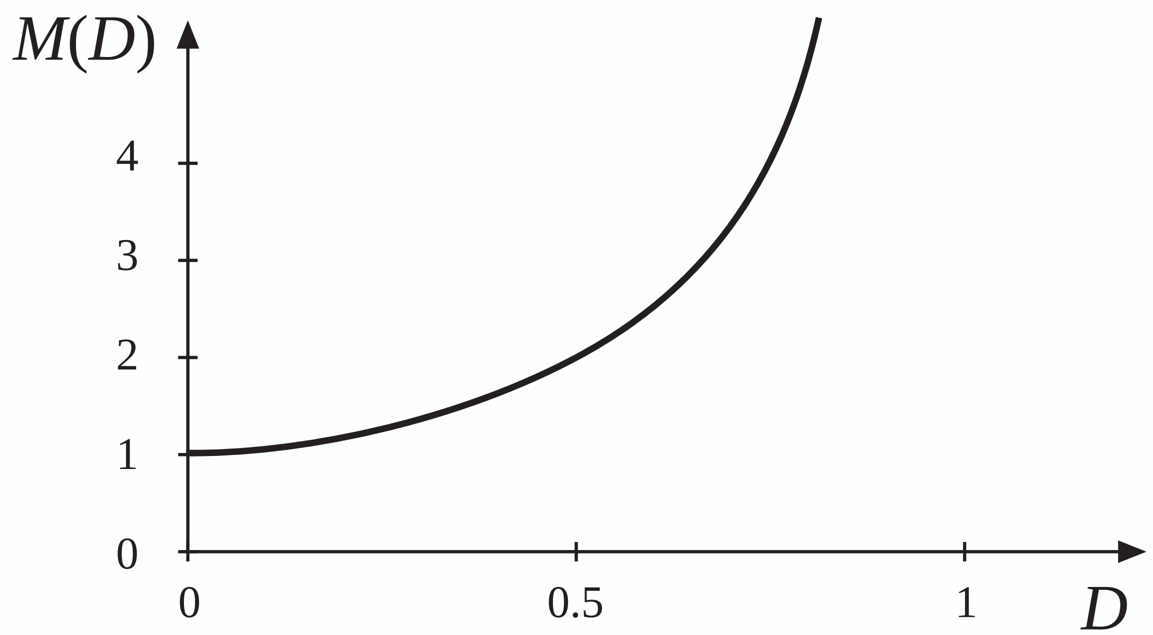
1. *Buck* $M(D) = D$





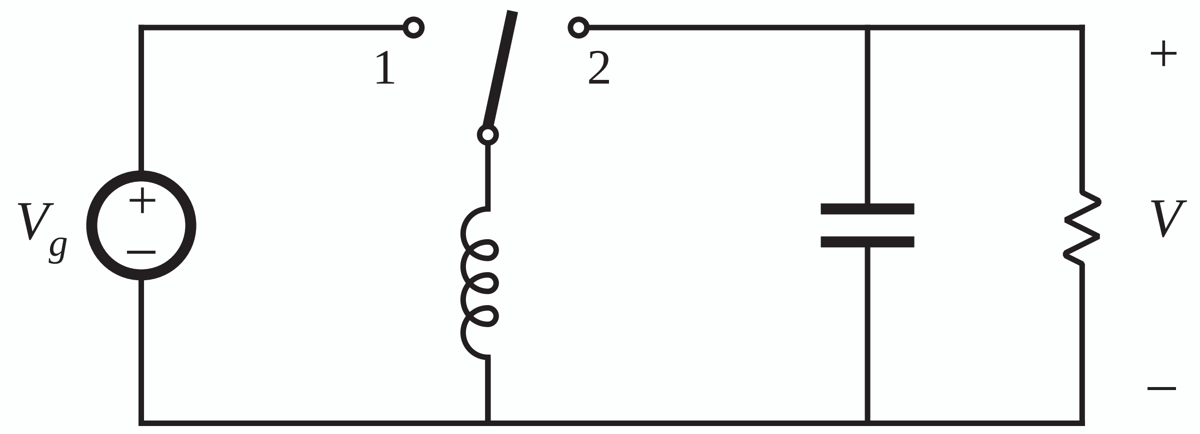
2. *Boost* $M(D) = \dfrac{1}{1-D}$

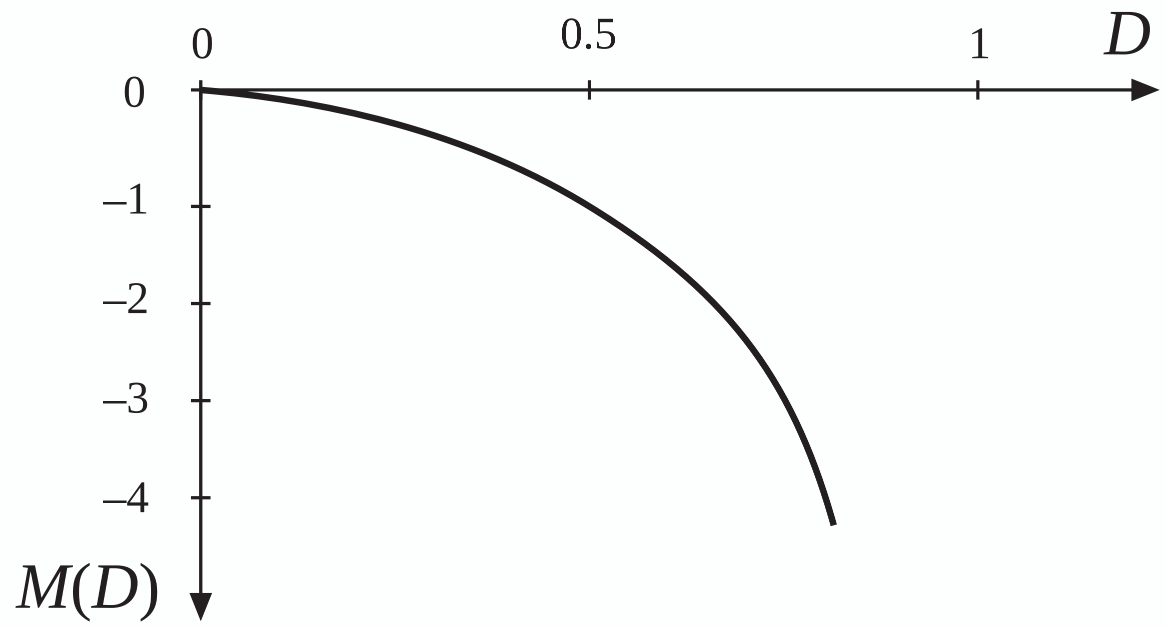




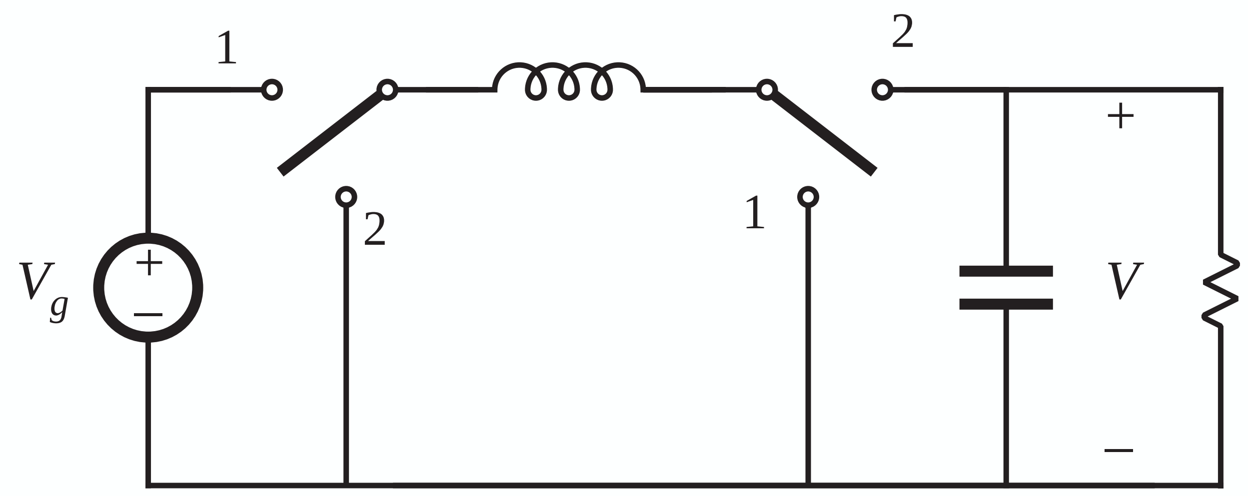
Converters producing a unipolar output voltage

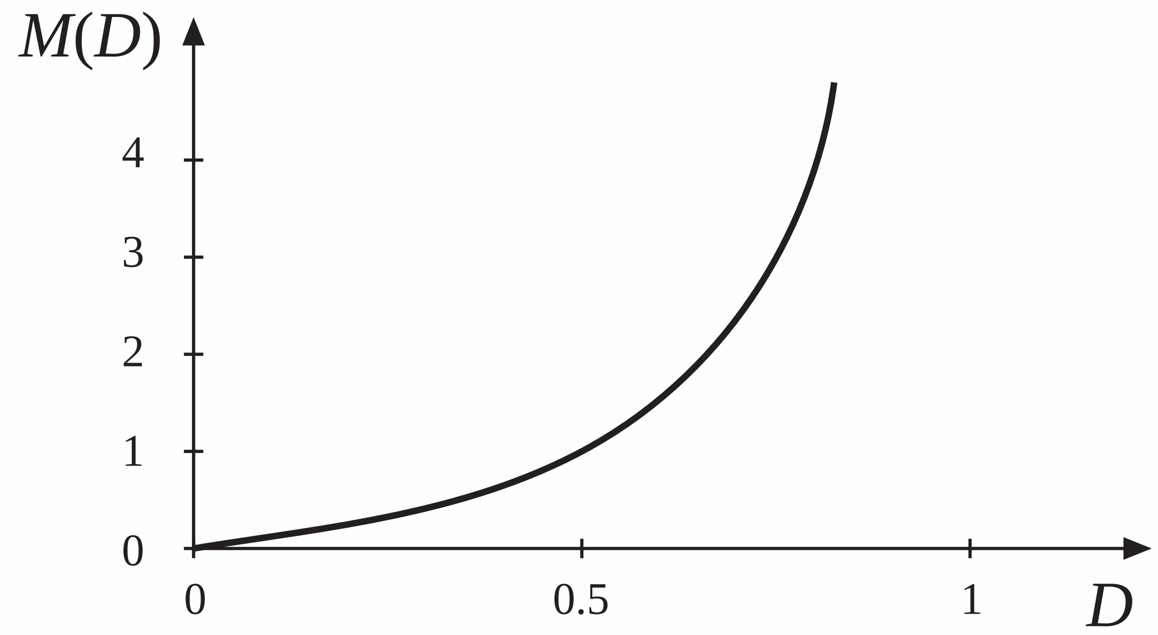
3. *Buck-boost* $\quad M(D) = -\dfrac{D}{1-D}$





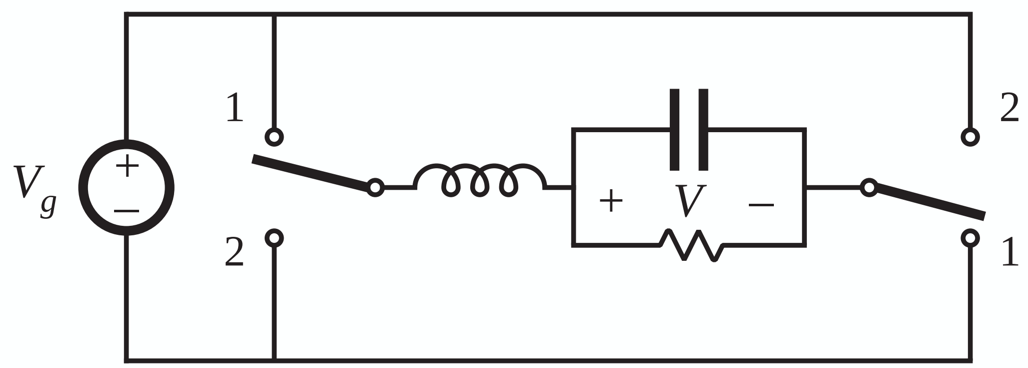
4. *Noninverting buck-boost* $\quad M(D) = \dfrac{D}{1-D}$

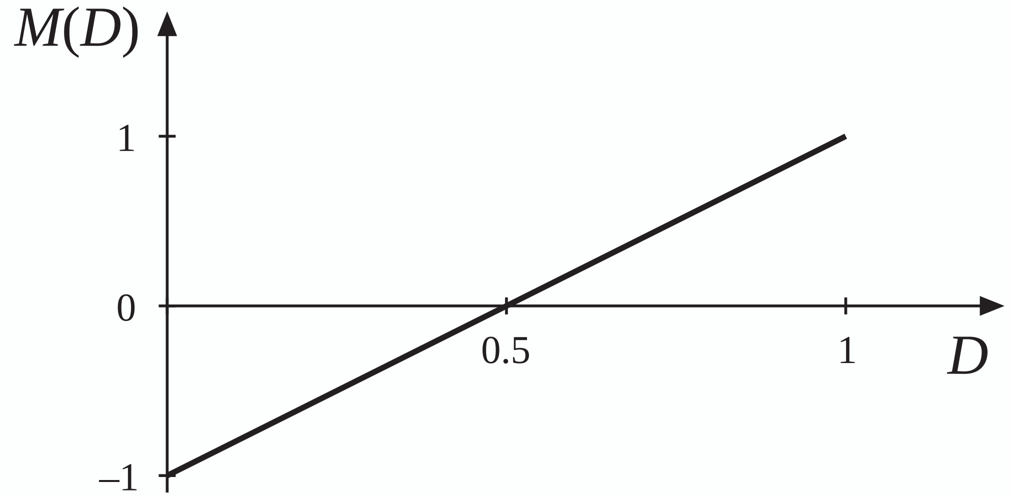




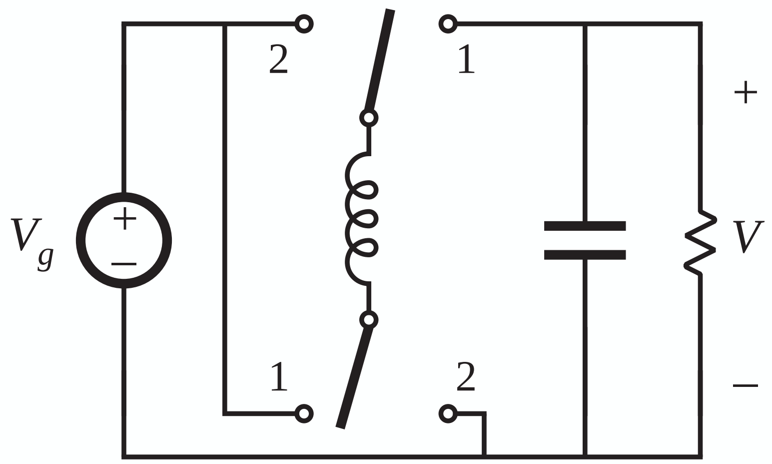
Converters producing a bipolar output voltage suitable as dc-ac inverters

5. *Bridge* $M(D) = 2D - 1$

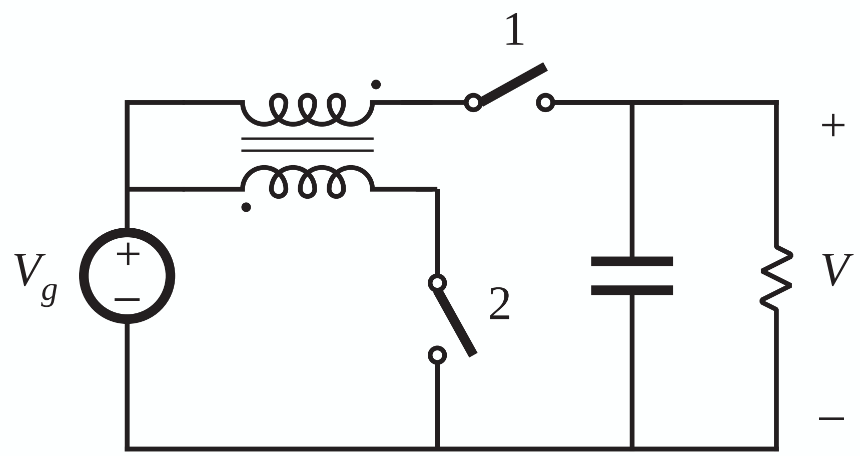


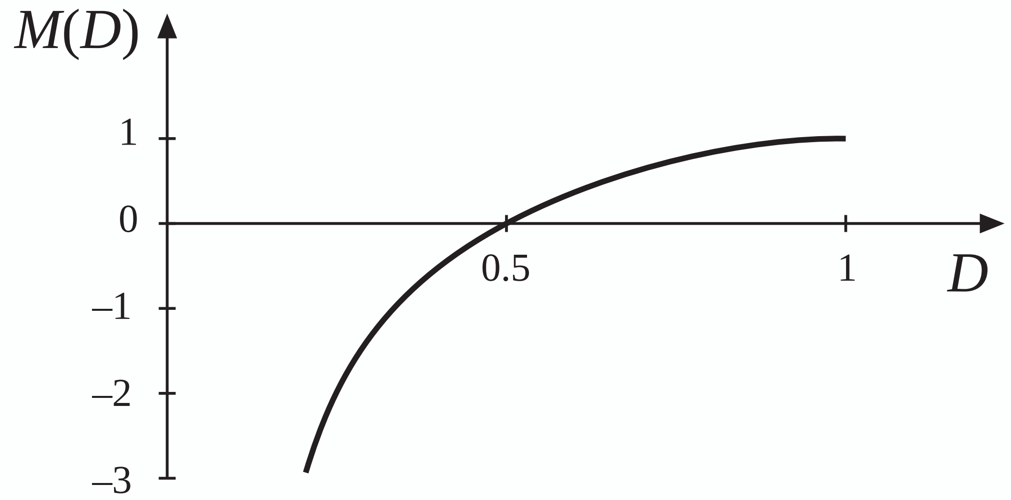


6. *Watkins-Johnson* $M(D) = \dfrac{2D-1}{D}$



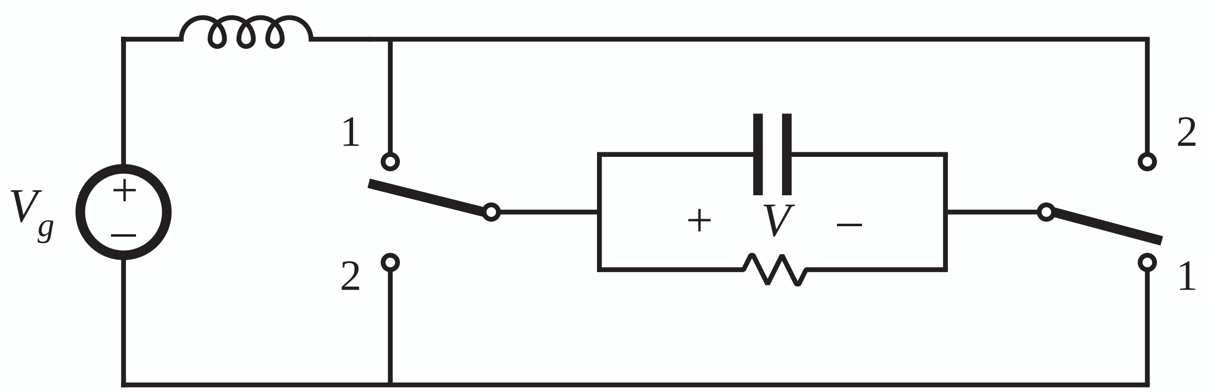
or

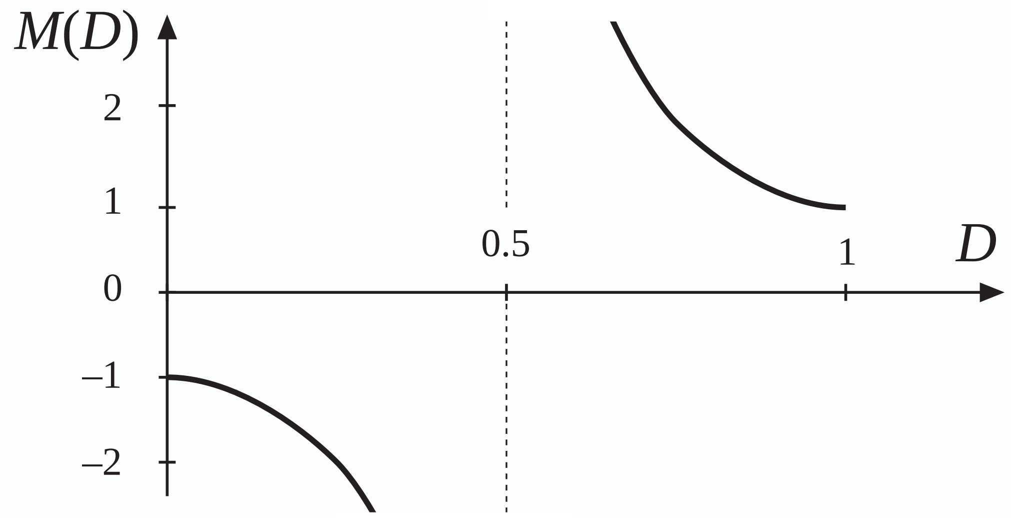




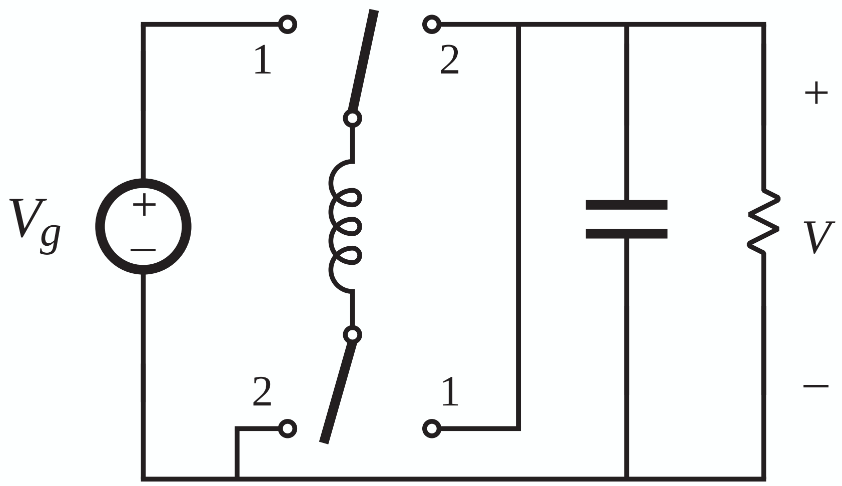
Converters producing a bipolar output voltage suitable as ac-dc rectifiers

7. *Current-fed bridge* $M(D) = \dfrac{1}{2D-1}$

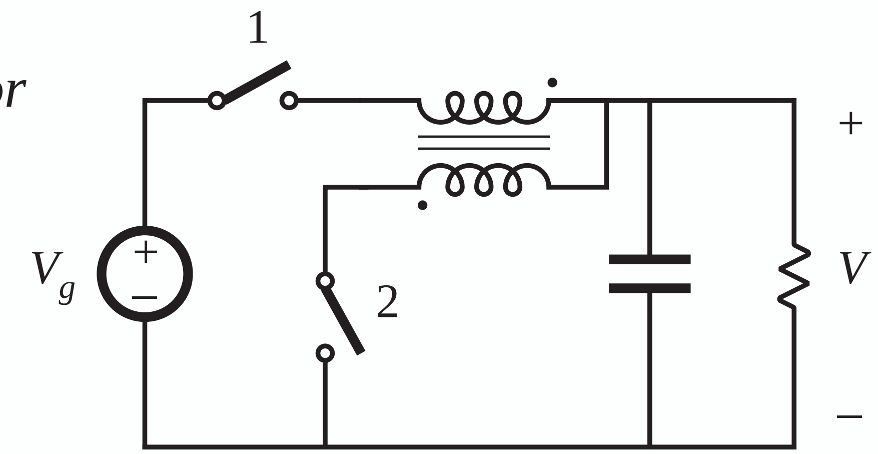


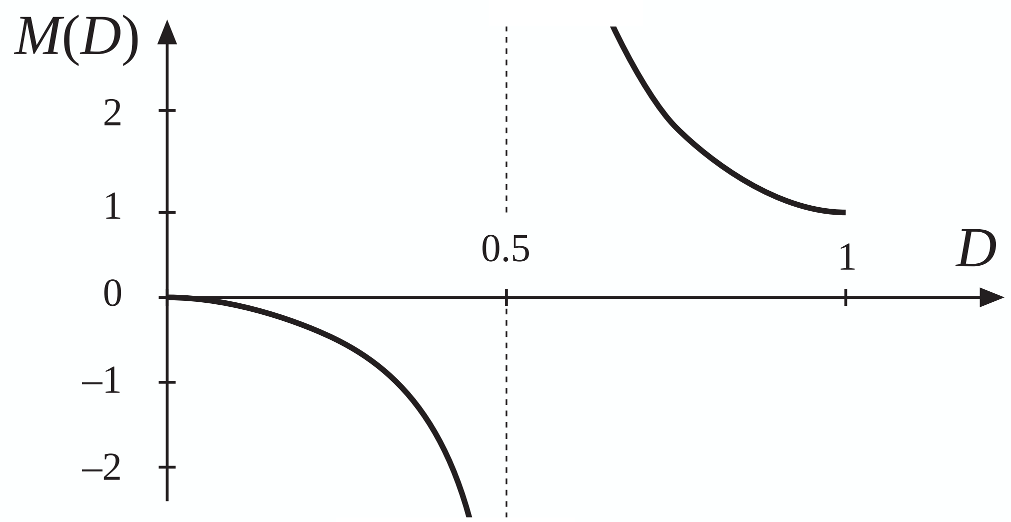


8. *Inverse of Watkins-Johnson* $M(D) = \dfrac{D}{2D-1}$



or

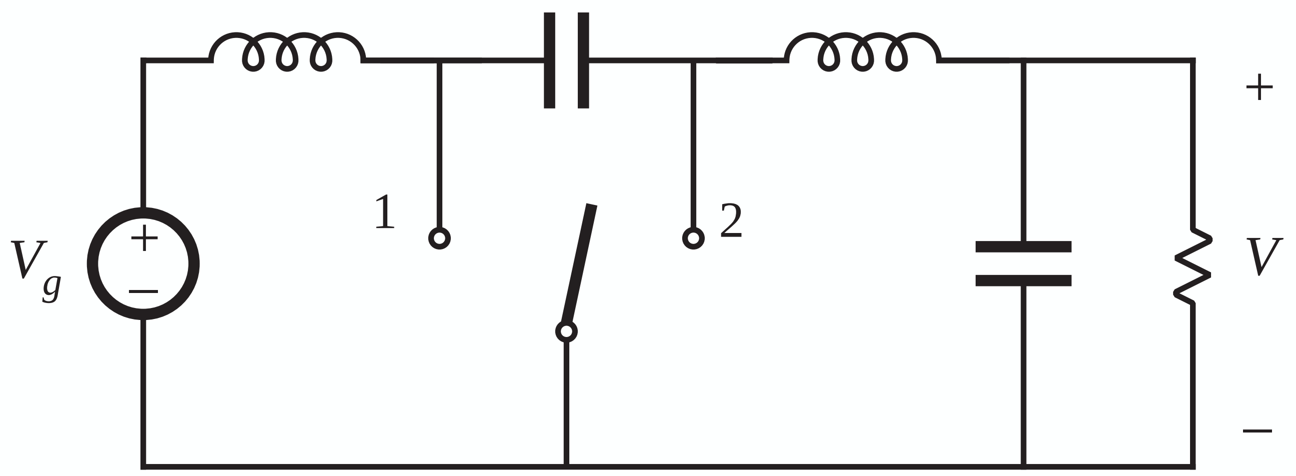


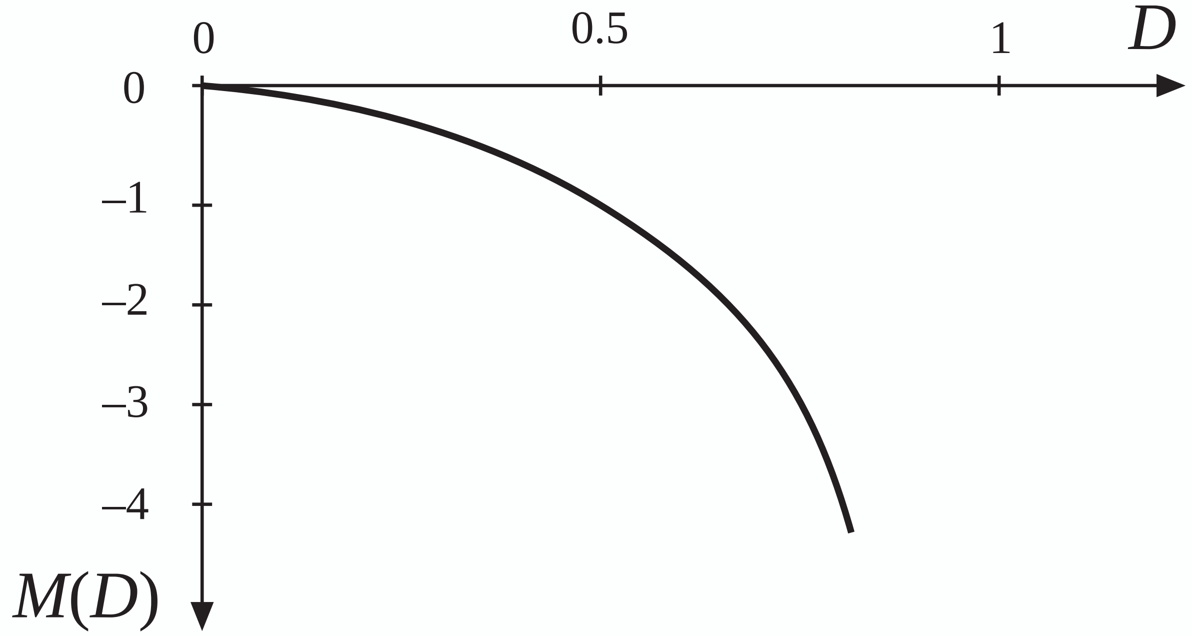


Several members of the class of two-inductor converters

1. *Ćuk*

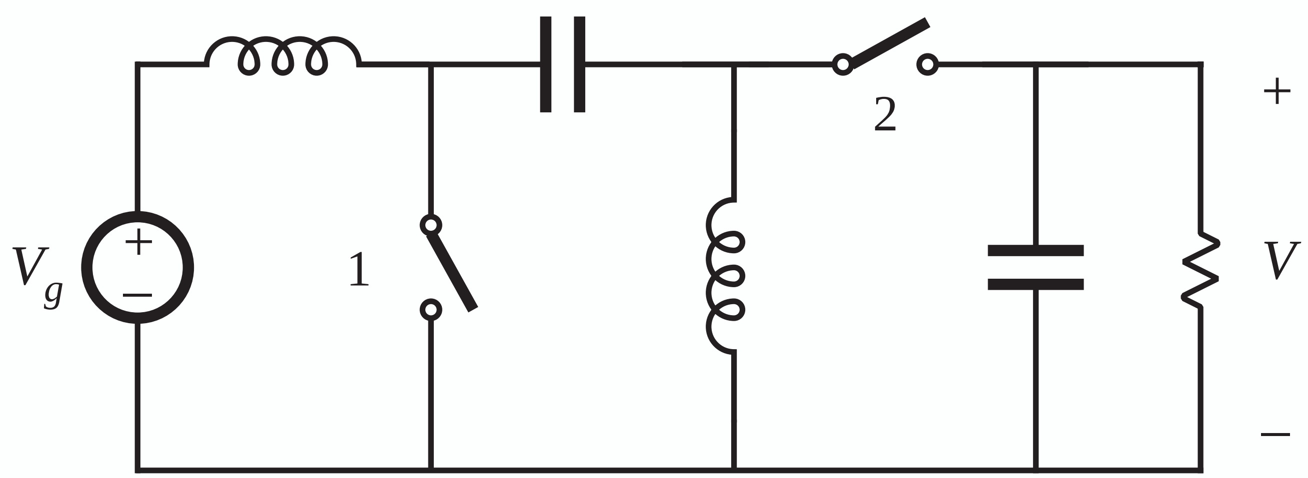
$$M(D) = -\frac{D}{1-D}$$

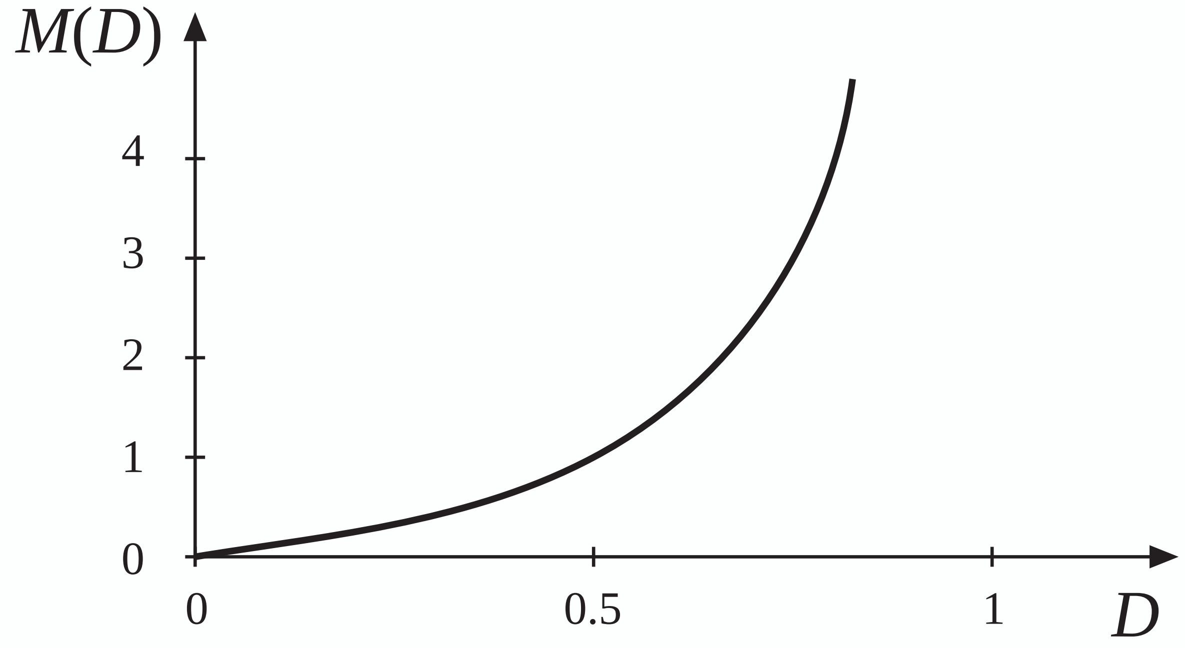




2. *SEPIC*

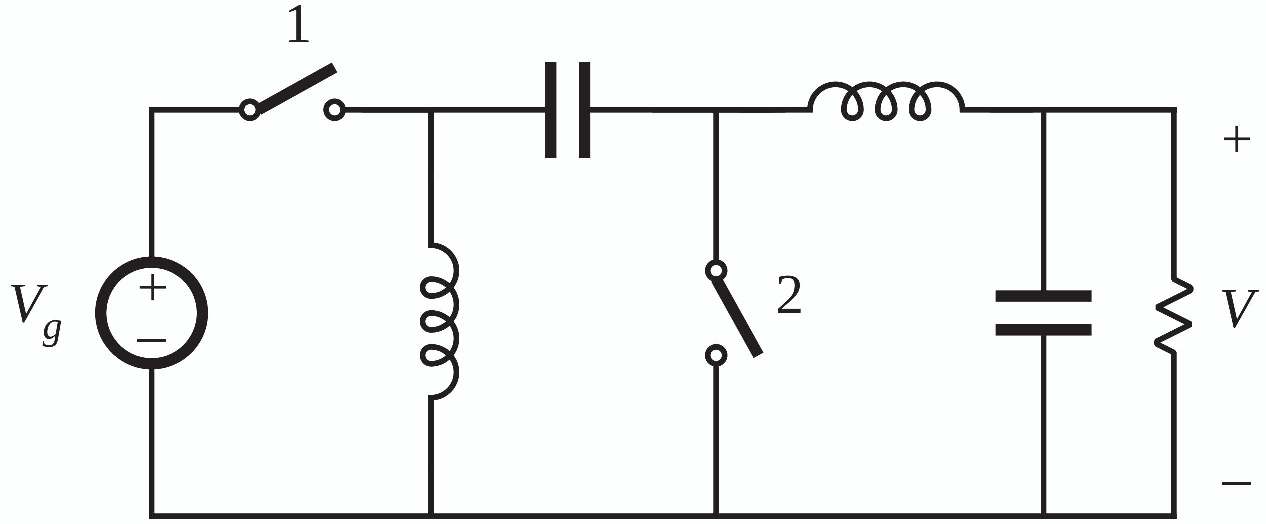
$$M(D) = \frac{D}{1-D}$$

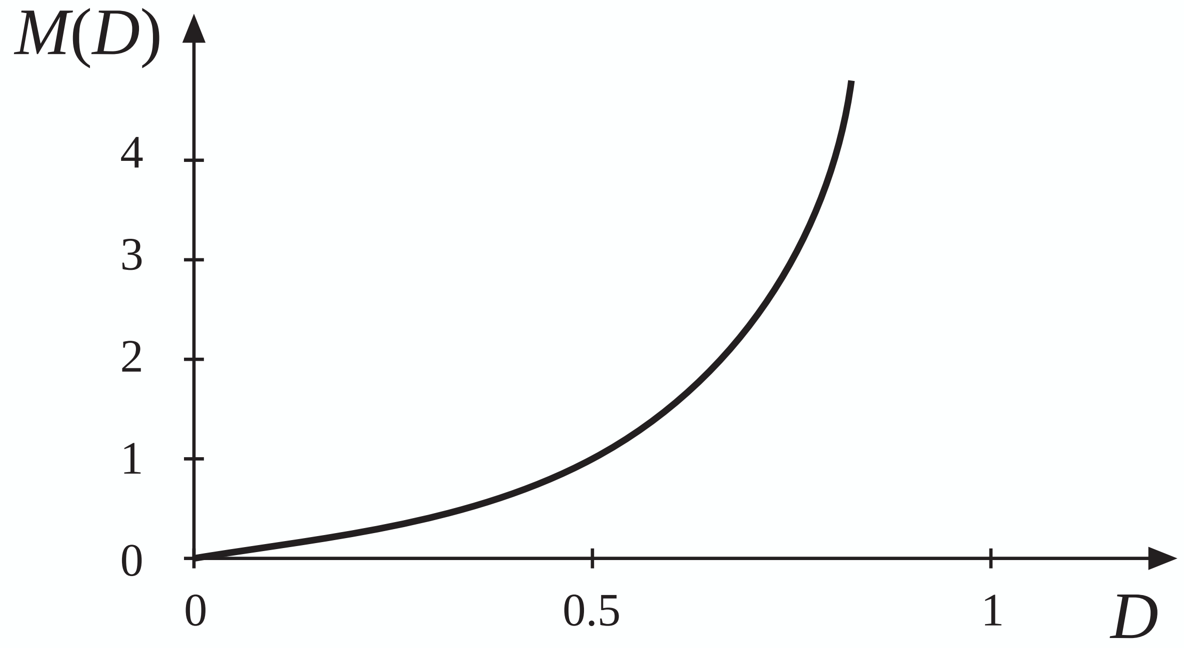




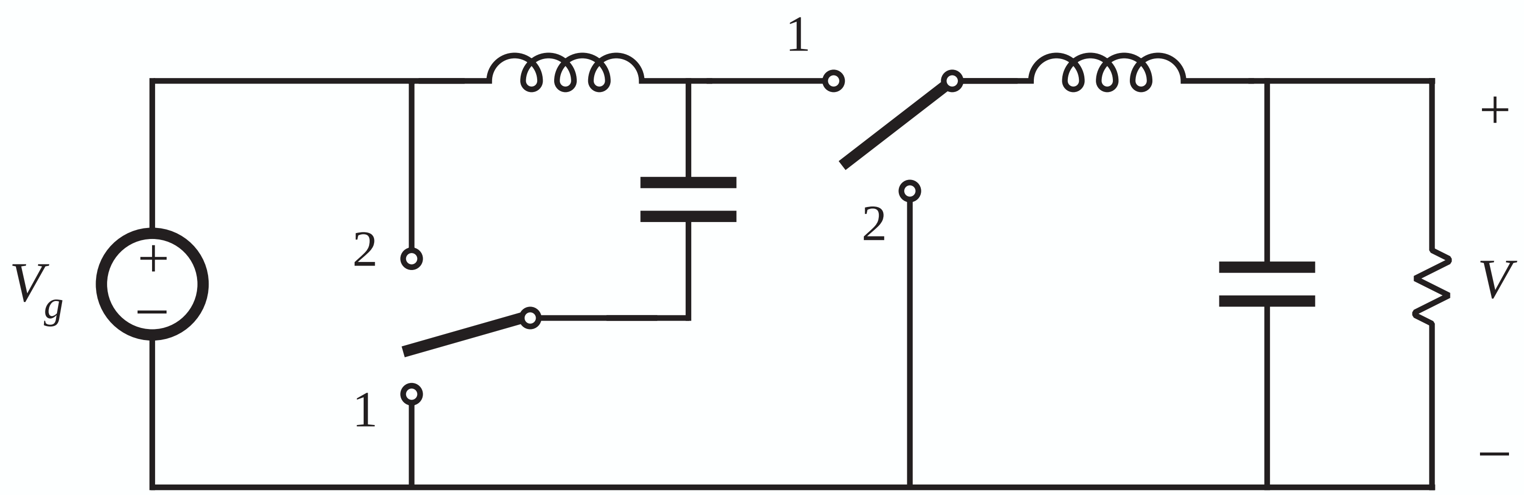
Several members of the class of two-inductor converters

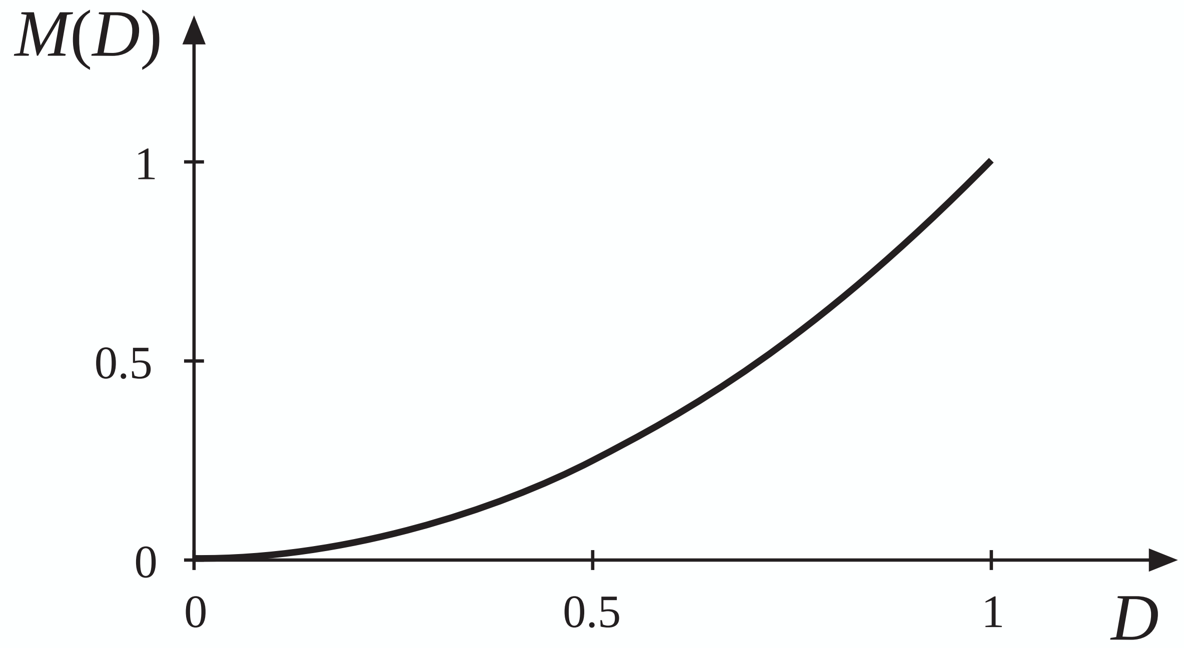
3. *Inverse of SEPIC* $\quad M(D) = \dfrac{D}{1-D}$





4. *Buck* ^{2} $\quad M(D) = D^2$





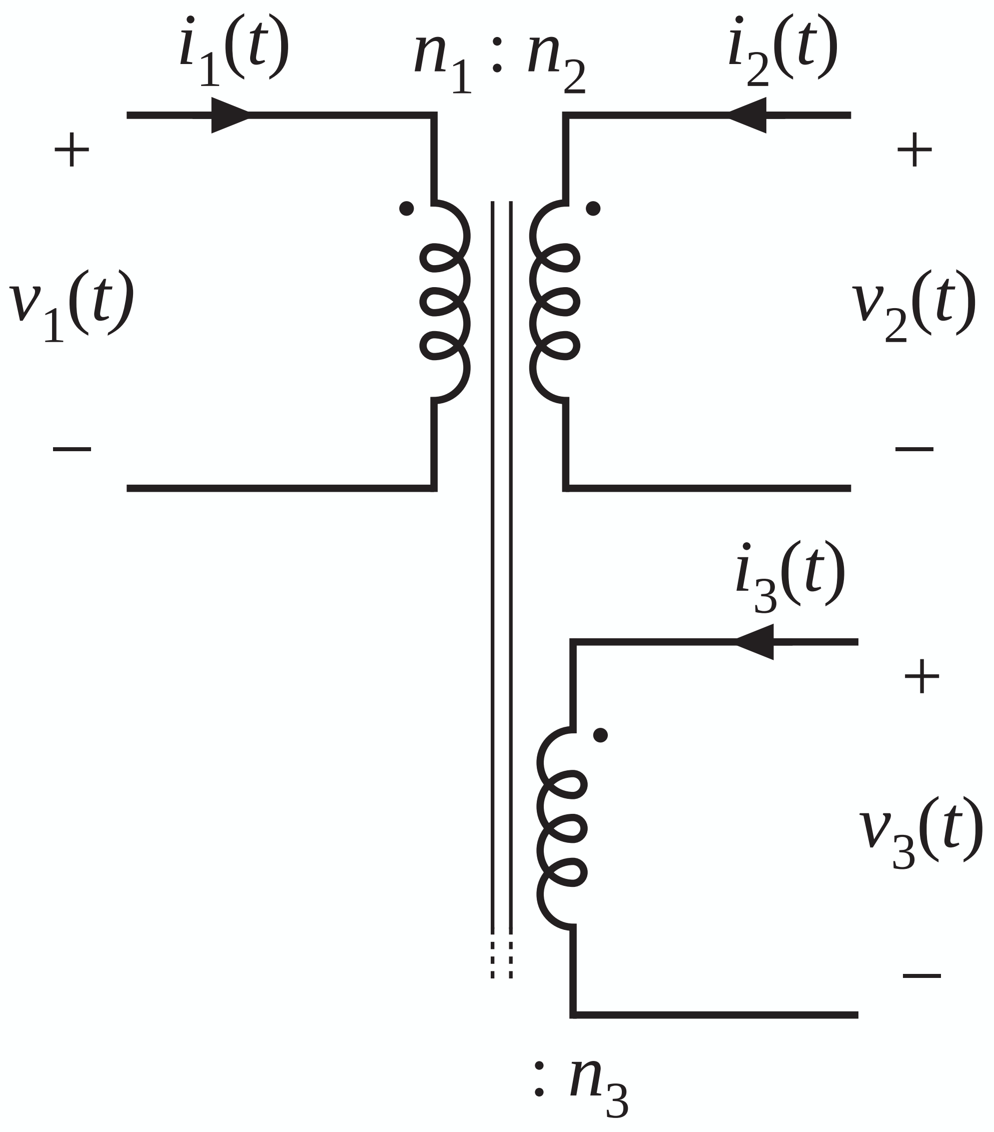
6.3. Transformer isolation

Objectives:

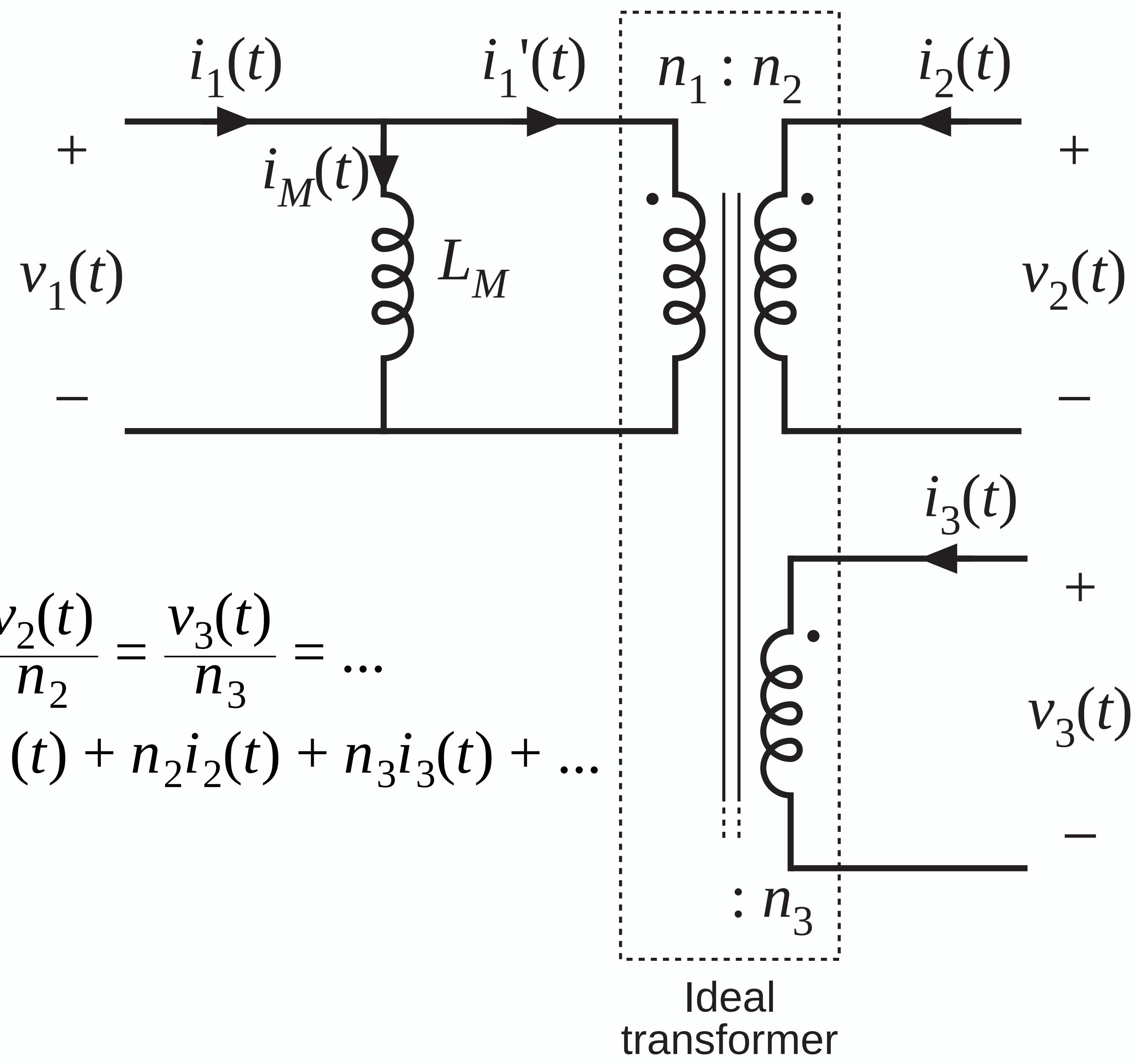
- Isolation of input and output ground connections, to meet safety requirements
- Reduction of transformer size by incorporating high frequency isolation transformer inside converter
- Minimization of current and voltage stresses when a large step-up or step-down conversion ratio is needed —use transformer turns ratio
- Obtain multiple output voltages via multiple transformer secondary windings and multiple converter secondary circuits

A simple transformer model

Multiple winding transformer



Equivalent circuit model



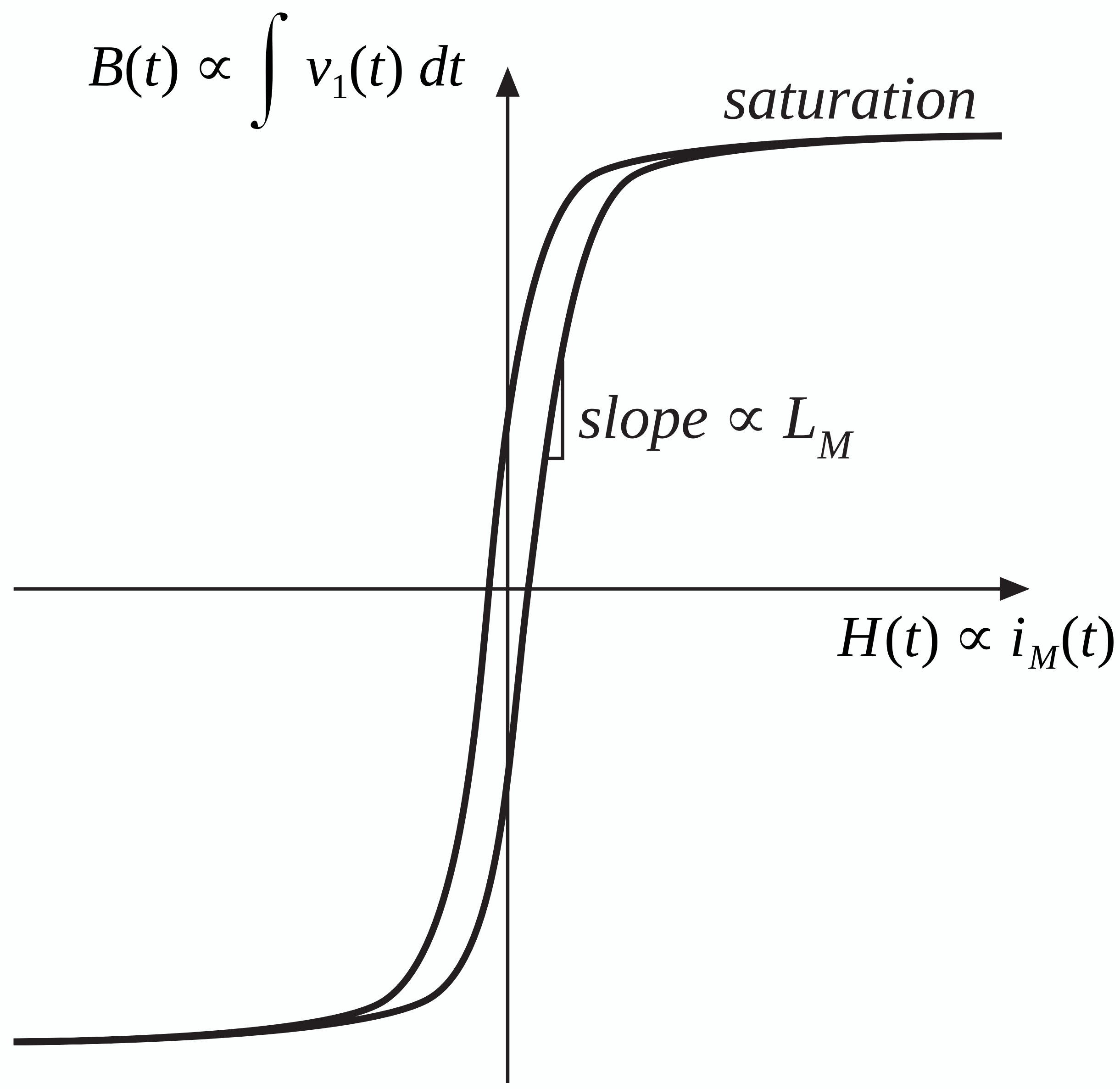
$$\frac{v_1(t)}{n_1} = \frac{v_2(t)}{n_2} = \frac{v_3(t)}{n_3} = \dots$$

$$0 = n_1 i_1'(t) + n_2 i_2(t) + n_3 i_3(t) + \dots$$

The magnetizing inductance L_M

- Models magnetization of transformer core material
- Appears effectively in parallel with windings
- If all secondary windings are disconnected, then primary winding behaves as an inductor, equal to the magnetizing inductance
- At dc: magnetizing inductance tends to short-circuit. Transformers cannot pass dc voltages
- Transformer saturates when magnetizing current i_M is too large

Transformer core B-H characteristic



Volt-second balance in L_M

The magnetizing inductance is a real inductor, obeying

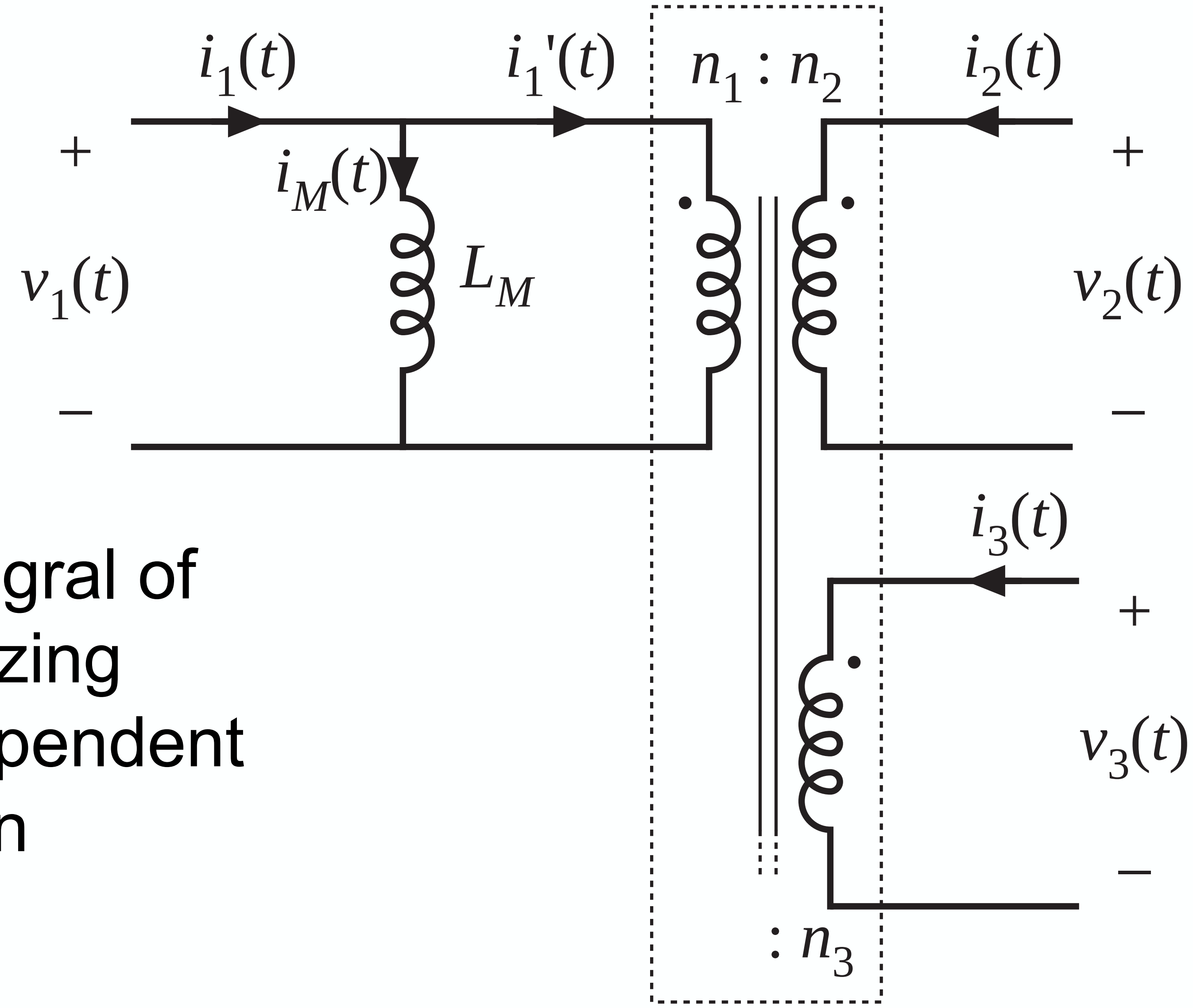
$$v_1(t) = L_M \frac{di_M(t)}{dt}$$

integrate:

$$i_M(t) - i_M(0) = \frac{1}{L_M} \int_0^t v_1(\tau)\, d\tau$$

Magnetizing current is determined by integral of the applied winding voltage. The magnetizing current and the winding currents are independent quantities. Volt-second balance applies: in steady-state, $i_M(T_s) = i_M(0)$, and hence

$$0 = \frac{1}{T_s} \int_0^{T_s} v_1(t)\, dt$$



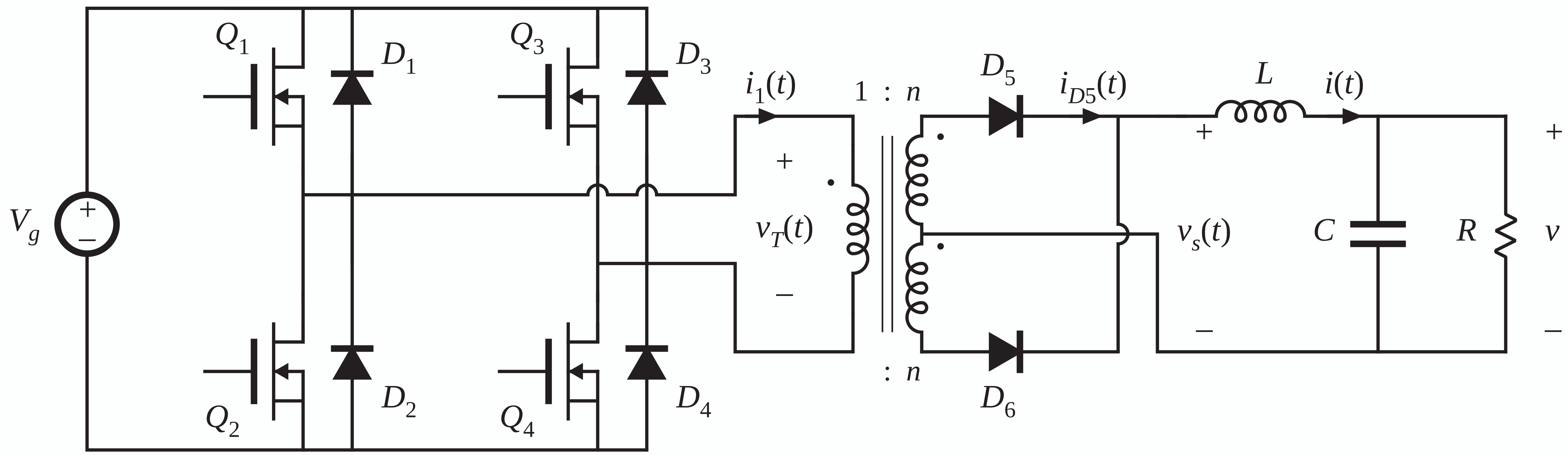
Ideal transformer

Transformer reset

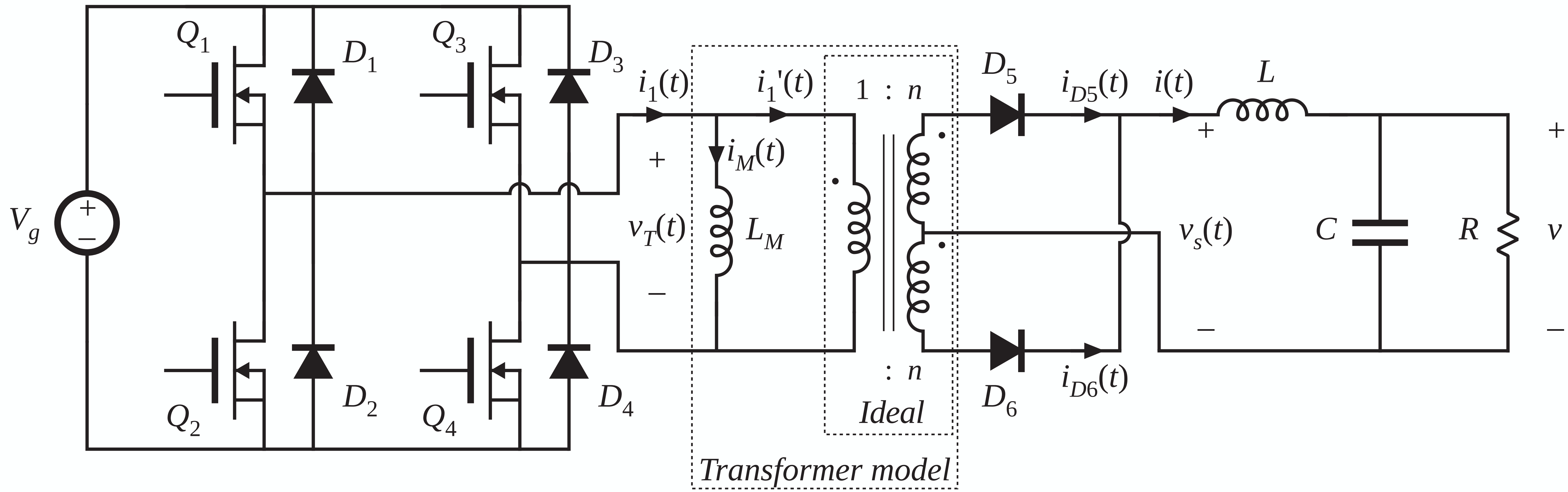
- "Transformer reset" is the mechanism by which magnetizing inductance volt-second balance is obtained
- The need to reset the transformer volt-seconds to zero by the end of each switching period adds considerable complexity to converters
- To understand operation of transformer-isolated converters:
    - replace transformer by equivalent circuit model containing magnetizing inductance
    - analyze converter as usual, treating magnetizing inductance as any other inductor
    - apply volt-second balance to all converter inductors, including magnetizing inductance

6.3.1. Full-bridge and half-bridge isolated buck converters

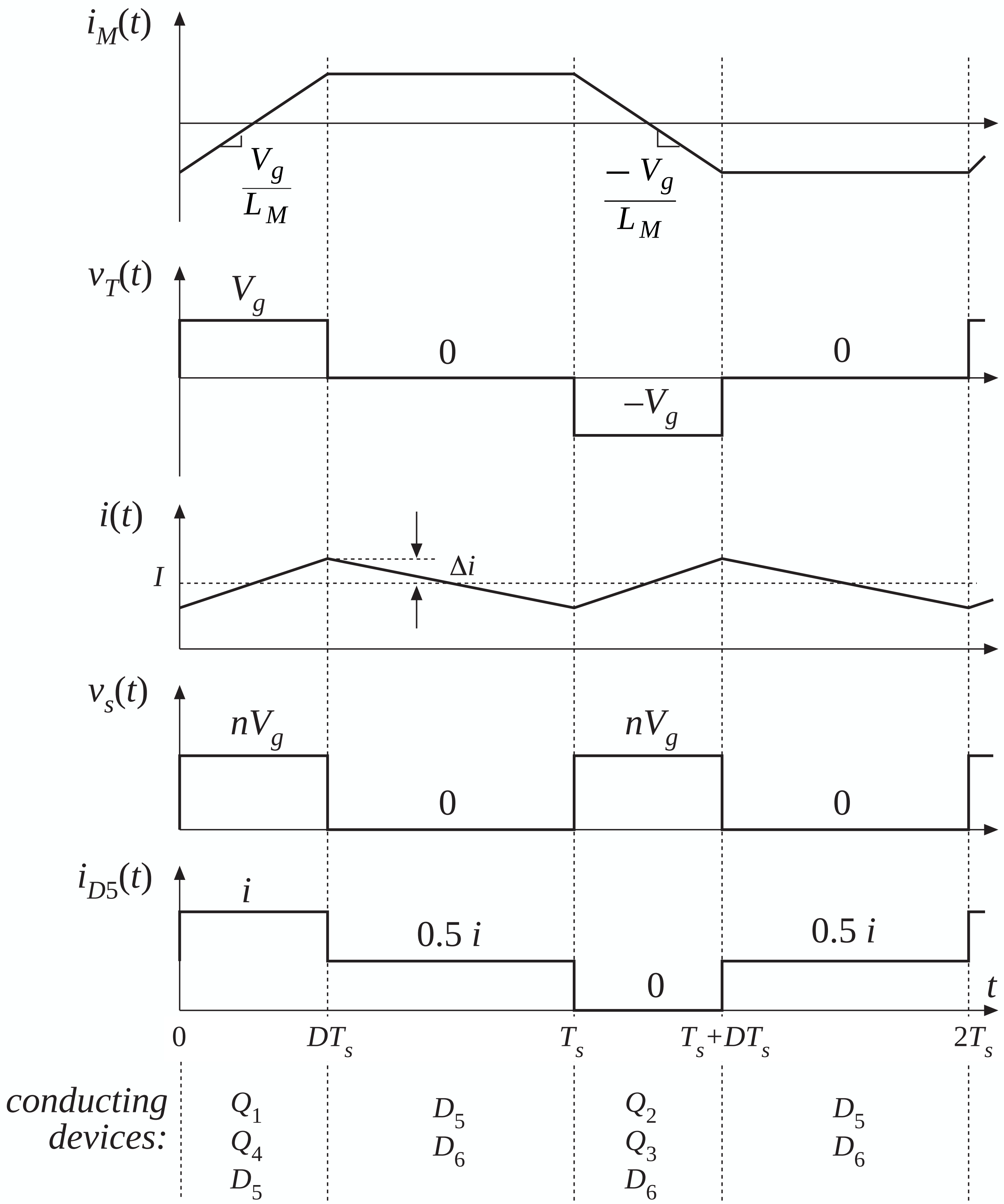
Full-bridge isolated buck converter



Full-bridge, with transformer equivalent circuit



Full-bridge: waveforms



- During first switching period: transistors Q_1 and Q_4 conduct for time DT_s , applying volt-seconds $V_g\ DT_s$ to primary winding
- During next switching period: transistors Q_2 and Q_3 conduct for time DT_s , applying volt-seconds $-V_g\ DT_s$ to primary winding
- Transformer volt-second balance is obtained over two switching periods
- Effect of nonidealities?

Effect of nonidealities on transformer volt-second balance

Volt-seconds applied to primary winding during first switching period:

$$(V_g - (Q_1 \text{ and } Q_4 \text{ forward voltage drops}))(Q_1 \text{ and } Q_4 \text{ conduction time})$$

Volt-seconds applied to primary winding during next switching period:

$$-(V_g - (Q_2 \text{ and } Q_3 \text{ forward voltage drops}))(Q_2 \text{ and } Q_3 \text{ conduction time})$$

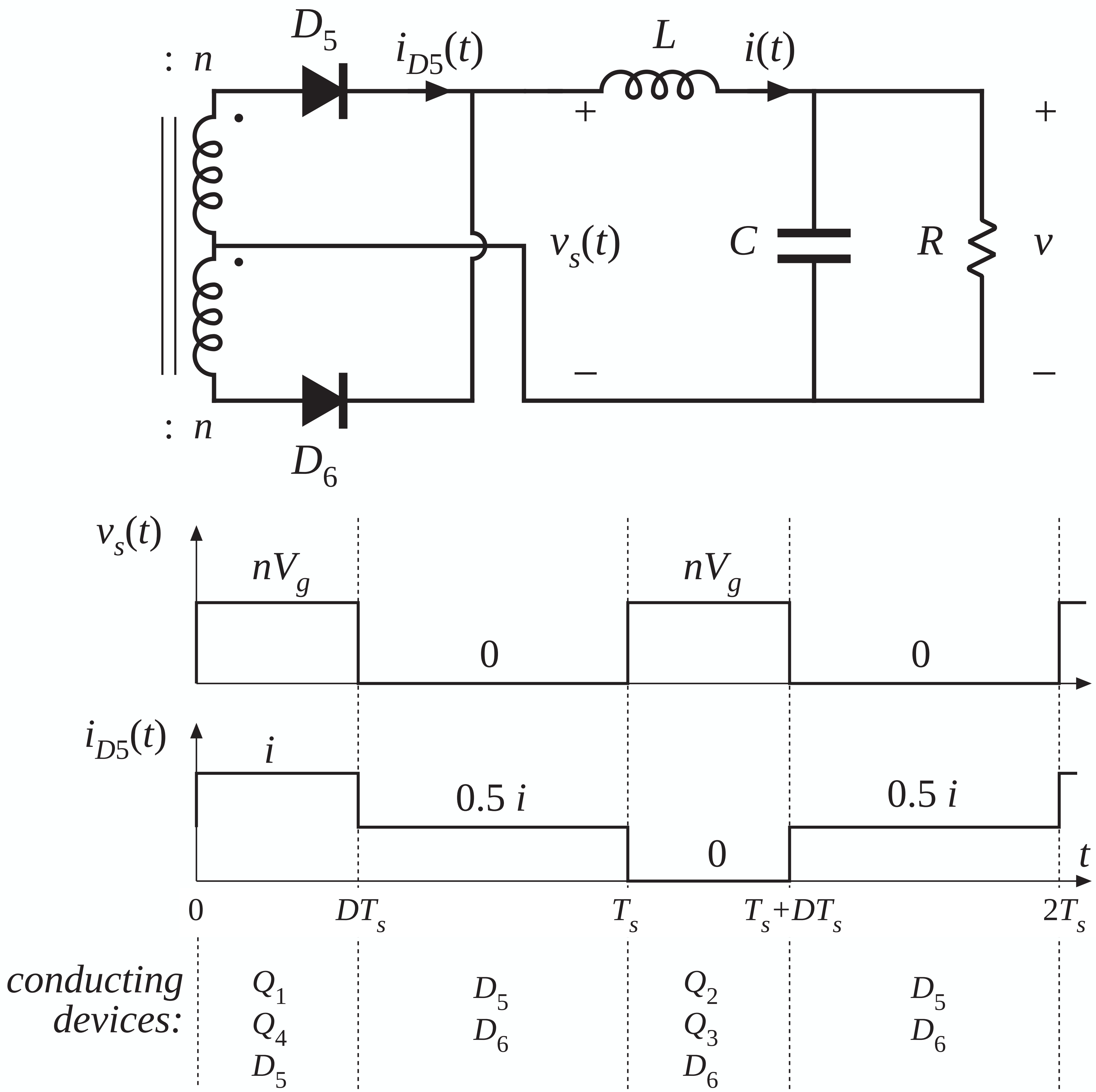
These volt-seconds never add to *exactly* zero.

Net volt-seconds are applied to primary winding

Magnetizing current slowly increases in magnitude

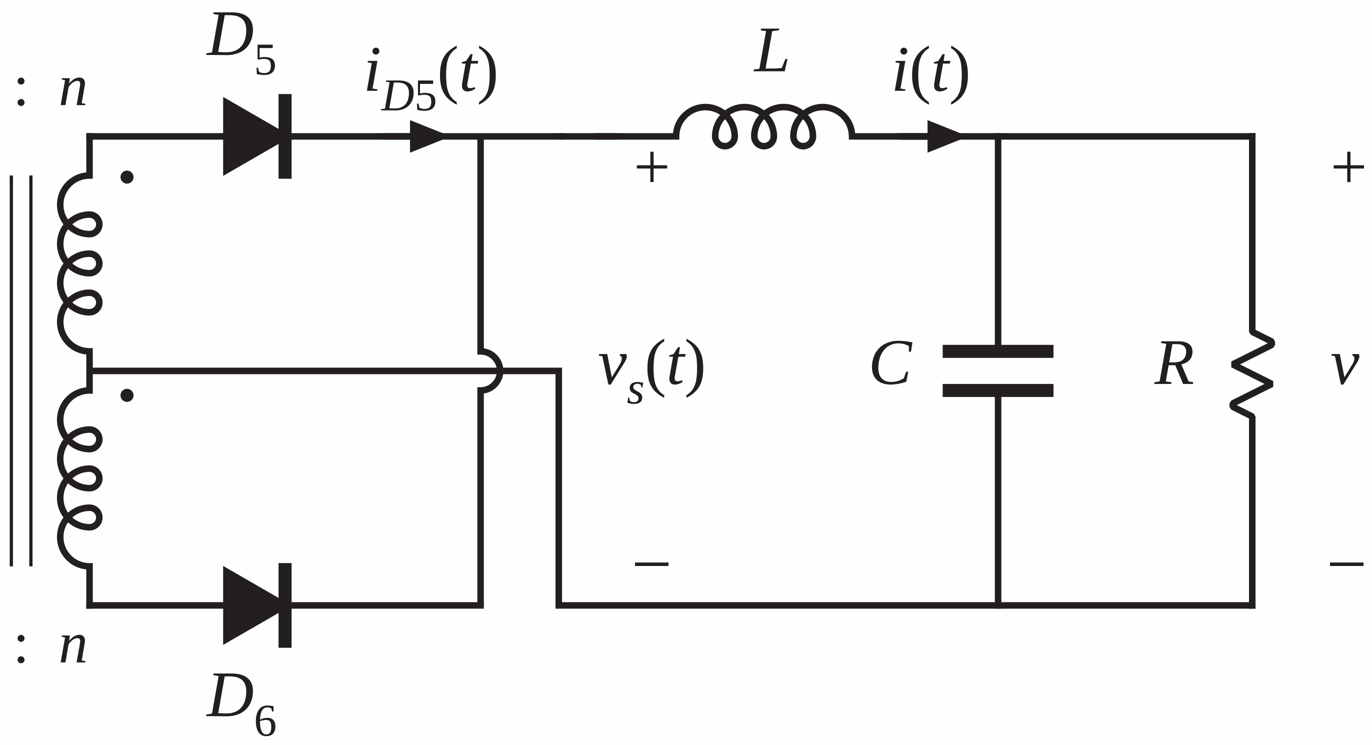
Saturation can be prevented by placing a capacitor in series with primary, or by use of current programmed mode (Chapter 12)

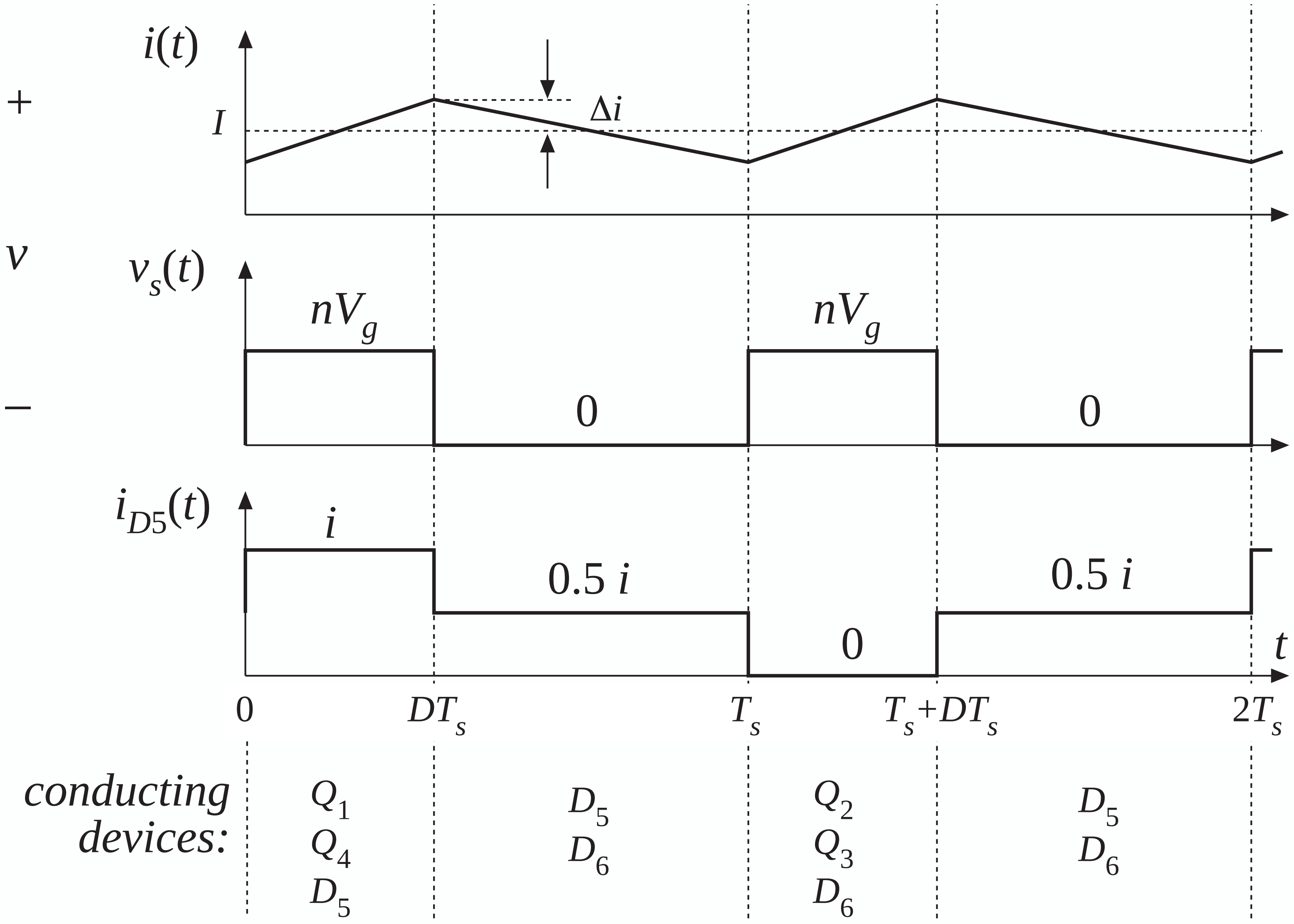
Operation of secondary-side diodes



- During second (D') subinterval, both secondary-side diodes conduct
- Output filter inductor current divides approximately equally between diodes
- Secondary amp-turns add to approximately zero
- Essentially no net magnetization of transformer core by secondary winding currents

Volt-second balance on output filter inductor



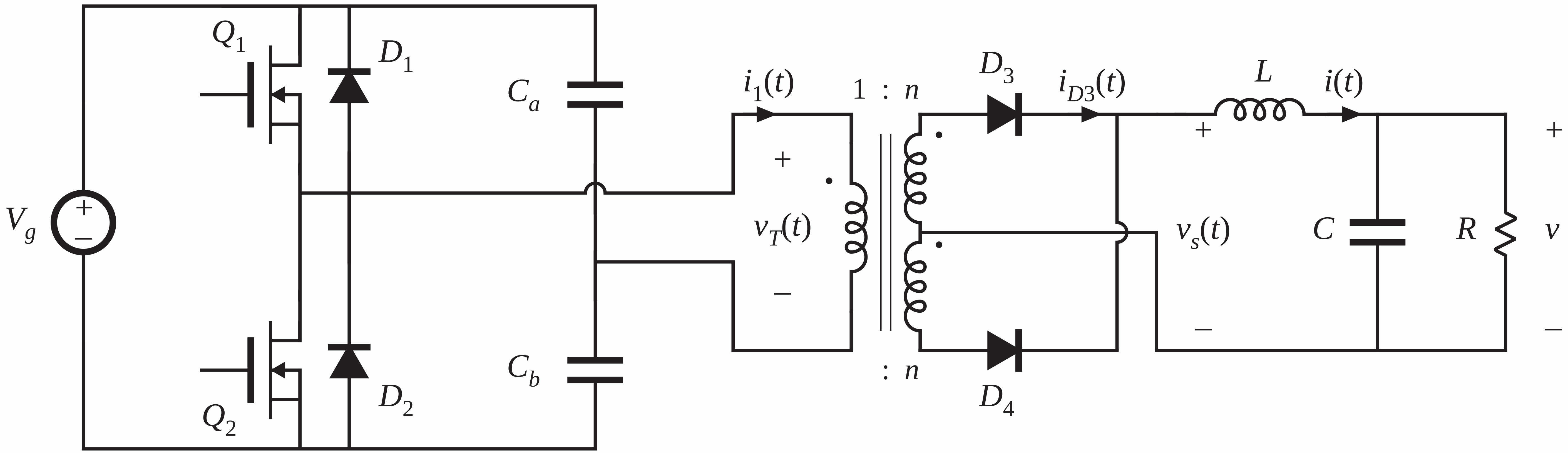


$$V = \left\langle v_s \right\rangle$$

$$V = nDV_g$$

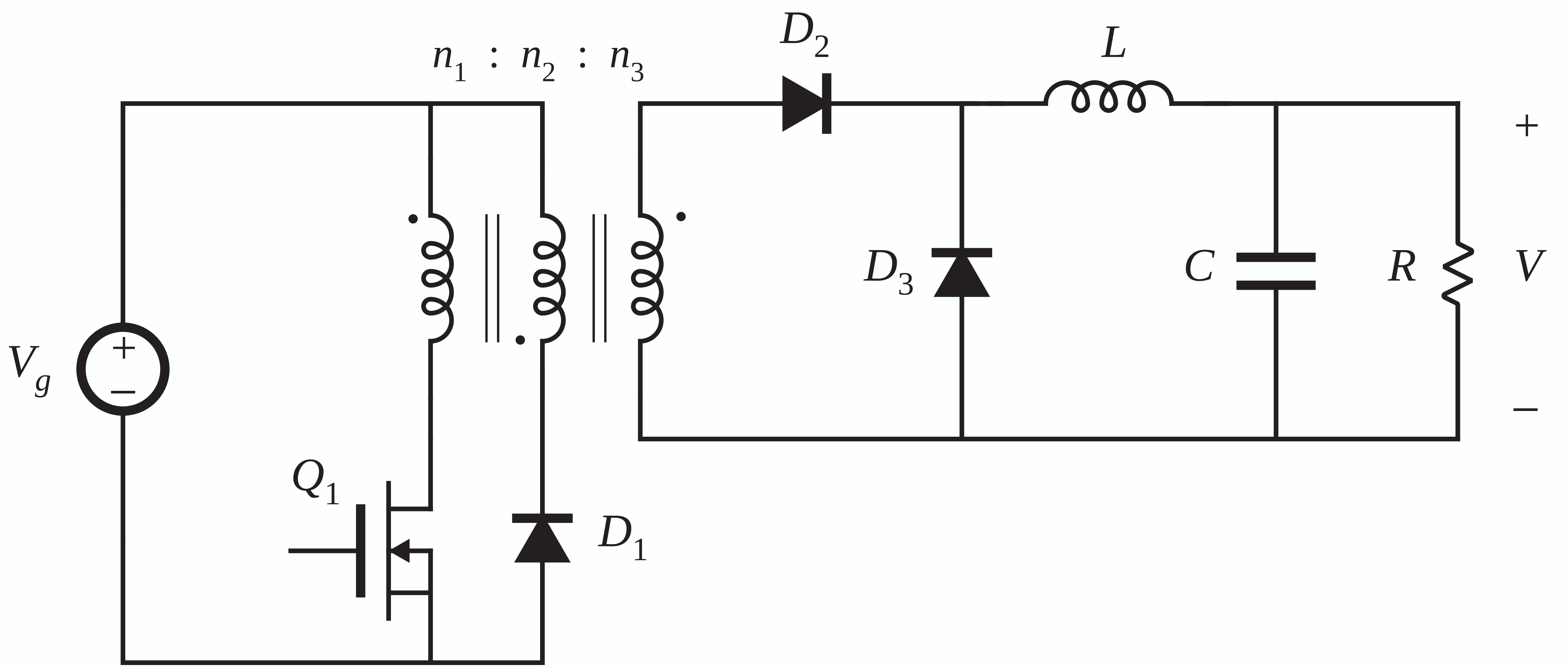
$$M(D) = nD \qquad \text{buck converter with turns ratio}$$

Half-bridge isolated buck converter



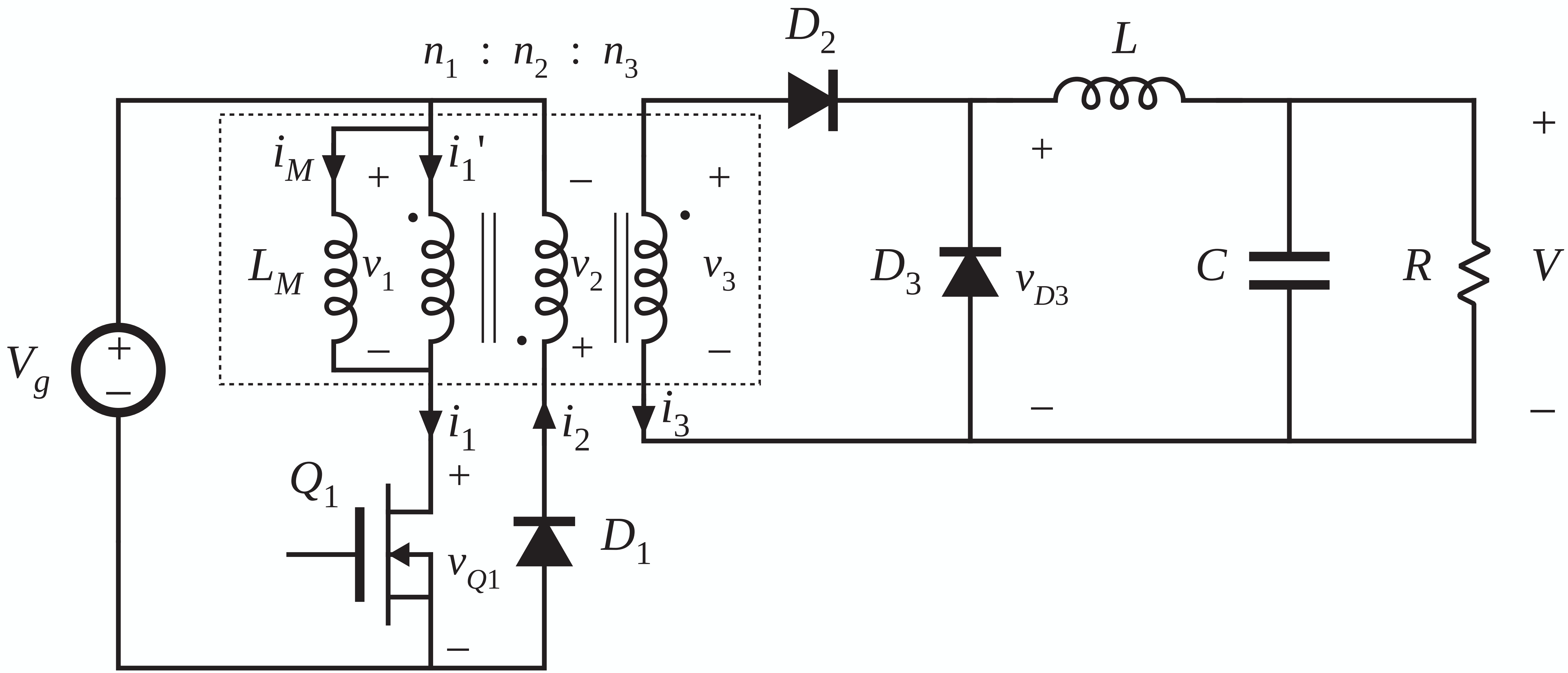
- Replace transistors Q_3 and Q_4 with large capacitors
- Voltage at capacitor centerpoint is $0.5V_g$
- $v_s(t)$ is reduced by a factor of two
- $M = 0.5\ nD$

6.3.2. Forward converter

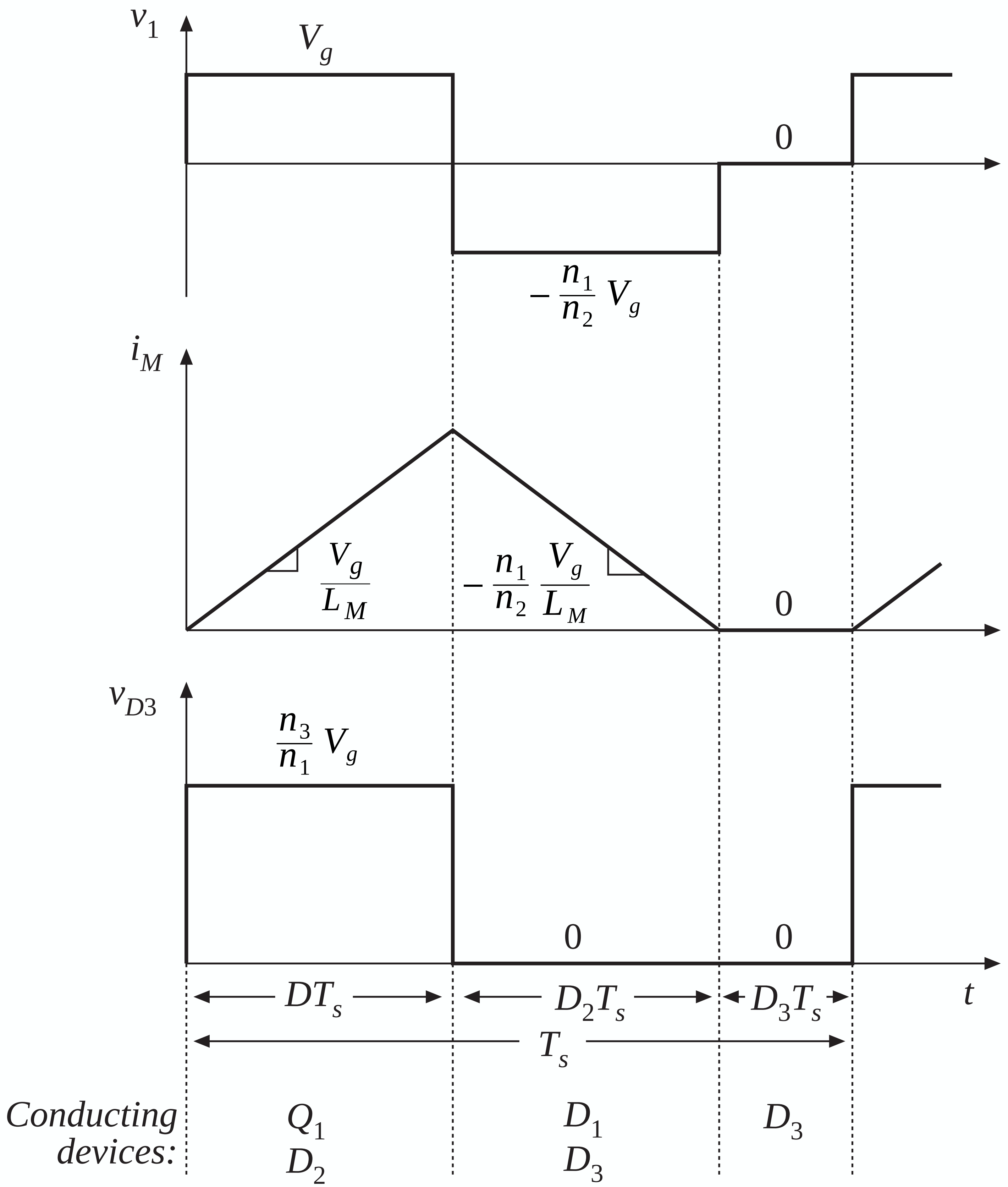


- Buck-derived transformer-isolated converter
- Single-transistor and two-transistor versions
- Maximum duty cycle is limited
- Transformer is reset while transistor is off

Forward converter with transformer equivalent circuit

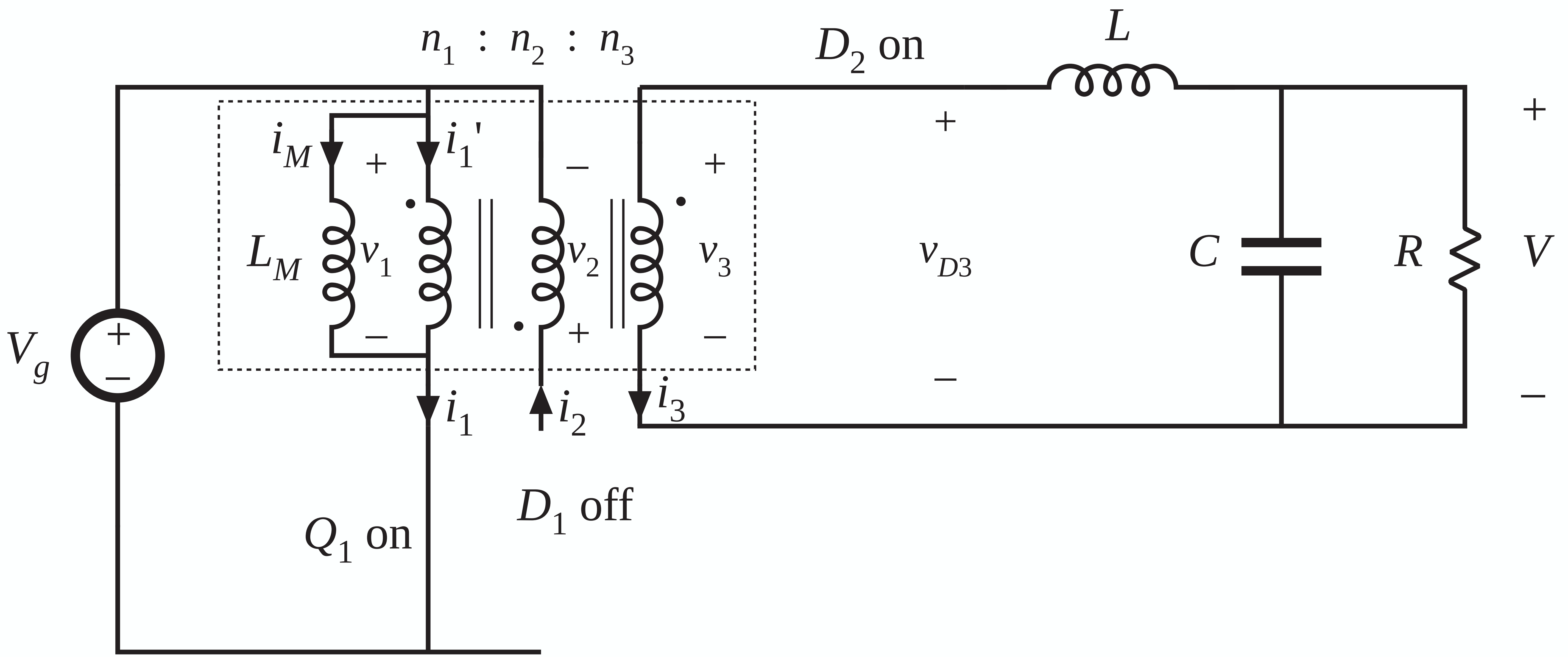


Forward converter: waveforms

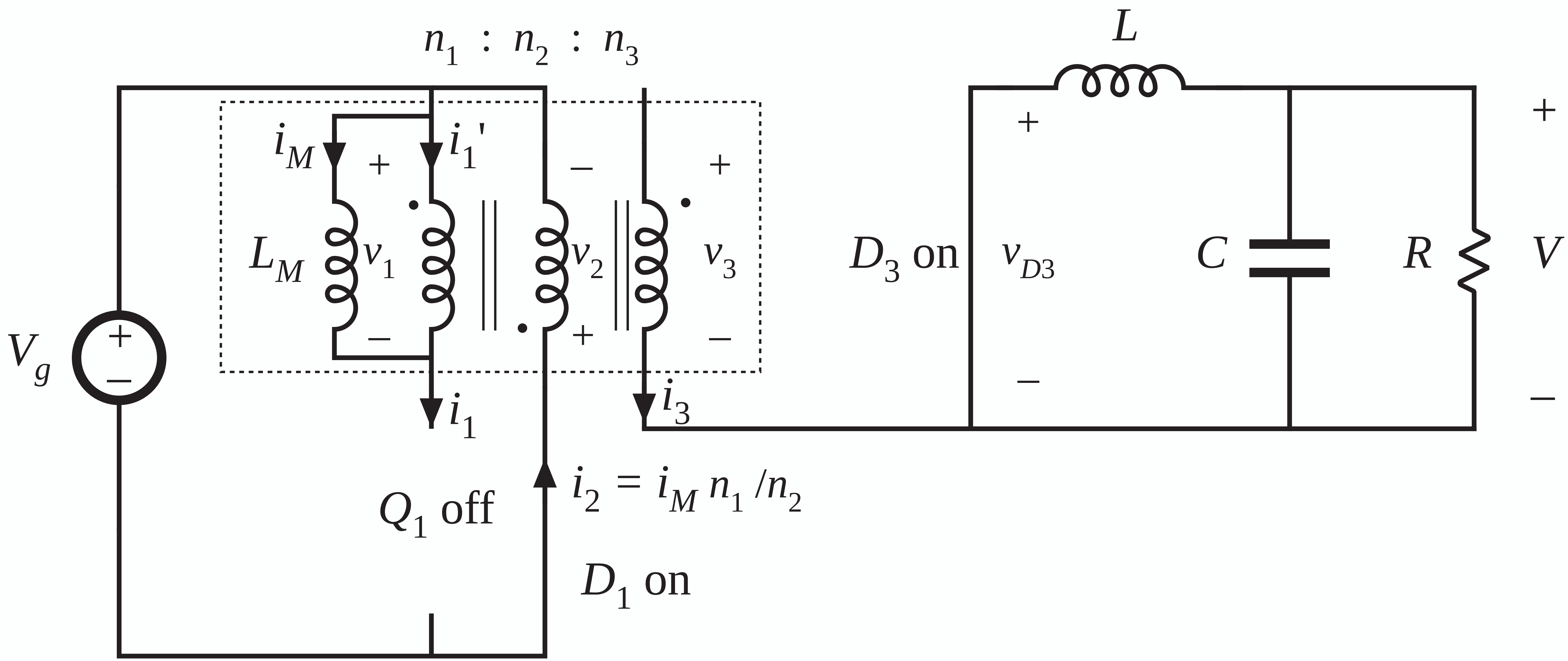


- Magnetizing current, in conjunction with diode D_1, operates in discontinuous conduction mode
- Output filter inductor, in conjunction with diode D_3, may operate in either CCM or DCM

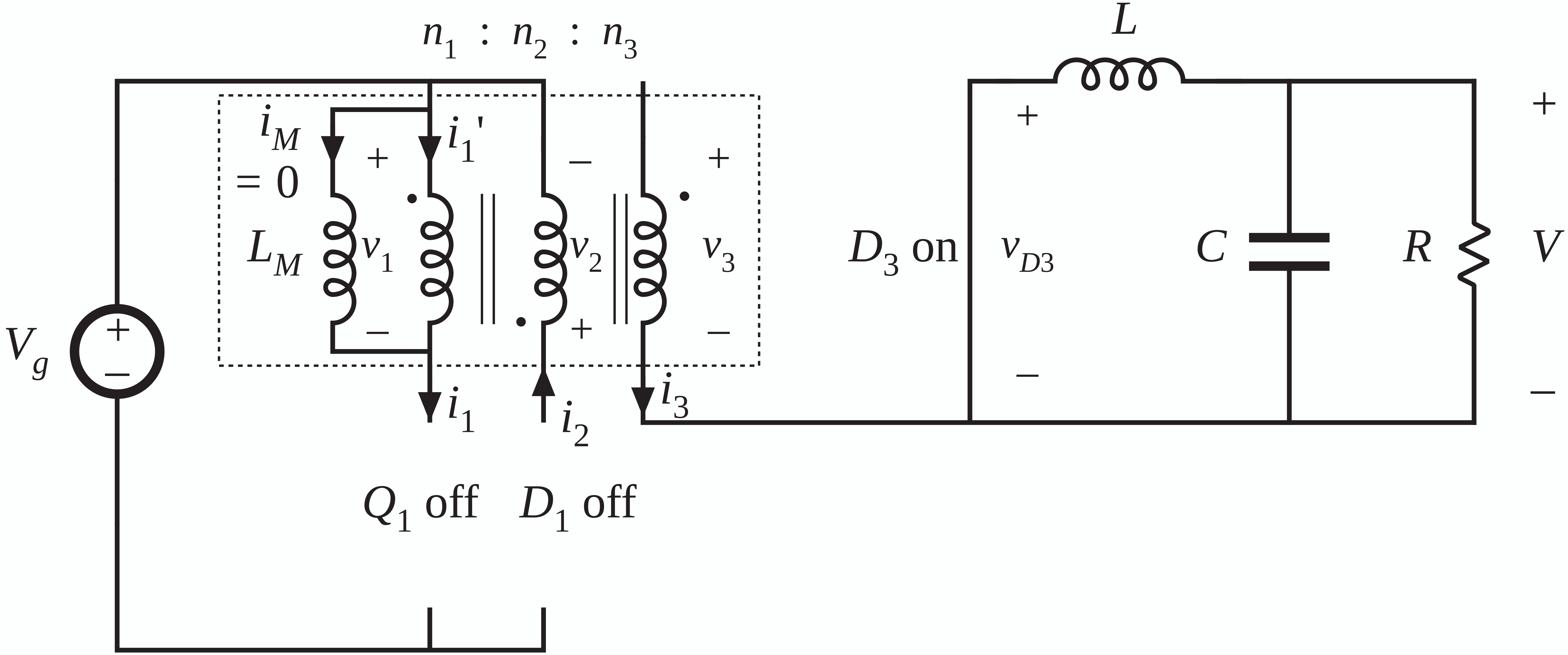
Subinterval 1: transistor conducts



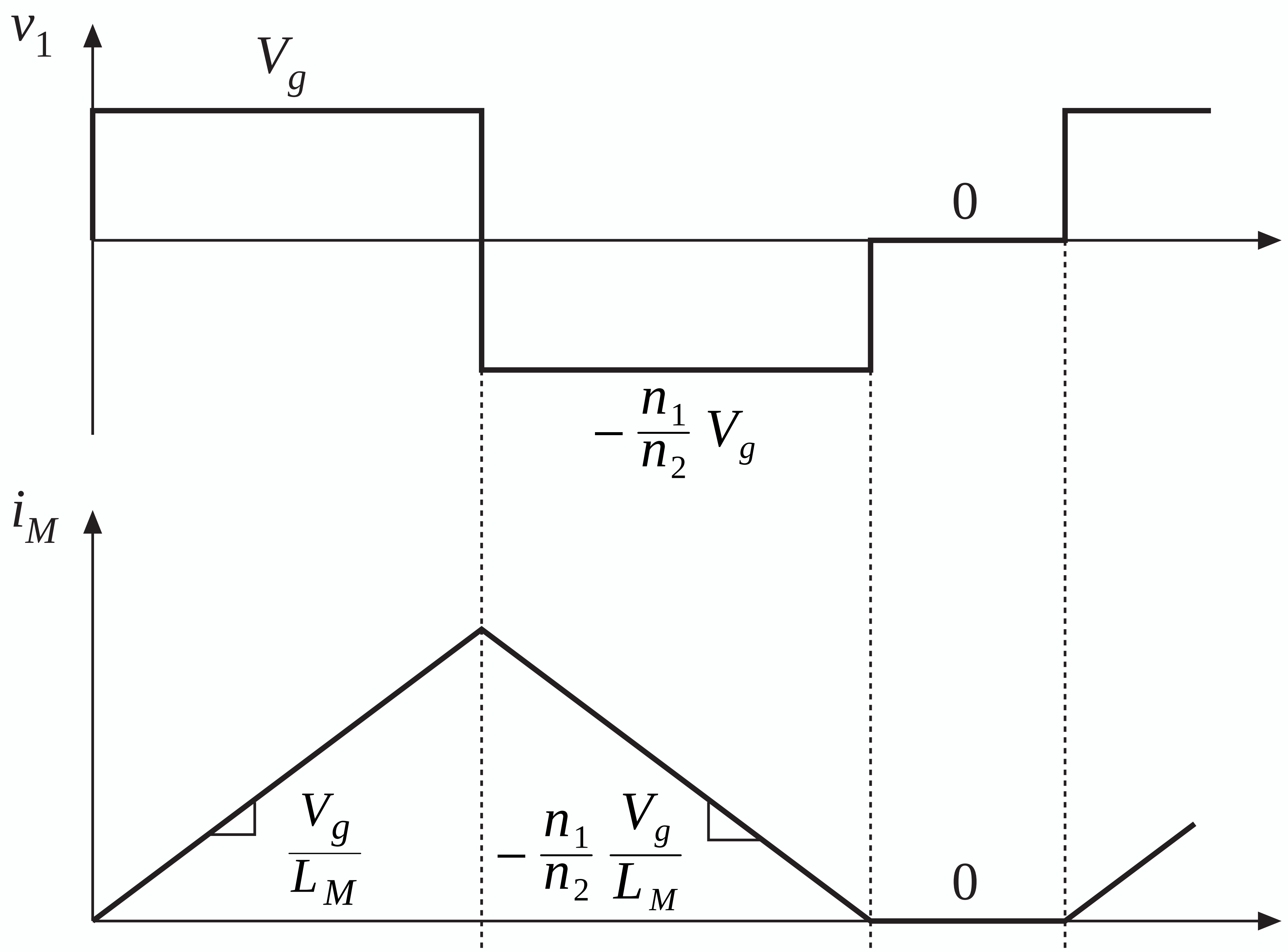
Subinterval 2: transformer reset



Subinterval 3



Magnetizing inductance volt-second balance



$$\left\langle v_1 \right\rangle = D\left(V_g\right) + D_2\left(-V_g n_1/n_2\right) + D_3\left(0\right) = 0$$

Transformer reset

From magnetizing current volt-second balance:

$$\langle v_1 \rangle = D\left(V_g\right) + D_2\left(-V_g n_1/n_2\right) + D_3\left(0\right) = 0$$

Solve for D_2:

$$D_2 = \frac{n_2}{n_1} D$$

D_3 cannot be negative. But $D_3 = 1 - D - D_2$. Hence

$$D_3 = 1 - D - D_2 \geq 0$$

$$D_3 = 1 - D\left(1 + \frac{n_2}{n_1}\right) \geq 0$$

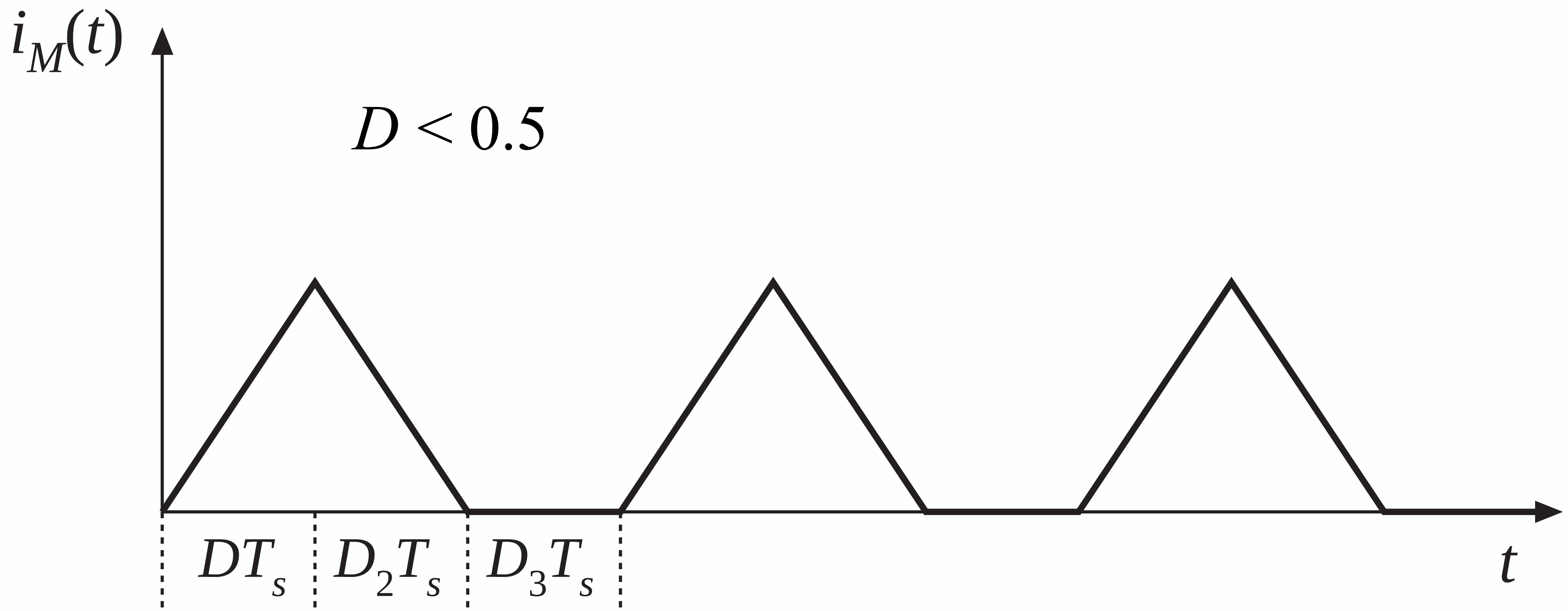
Solve for D

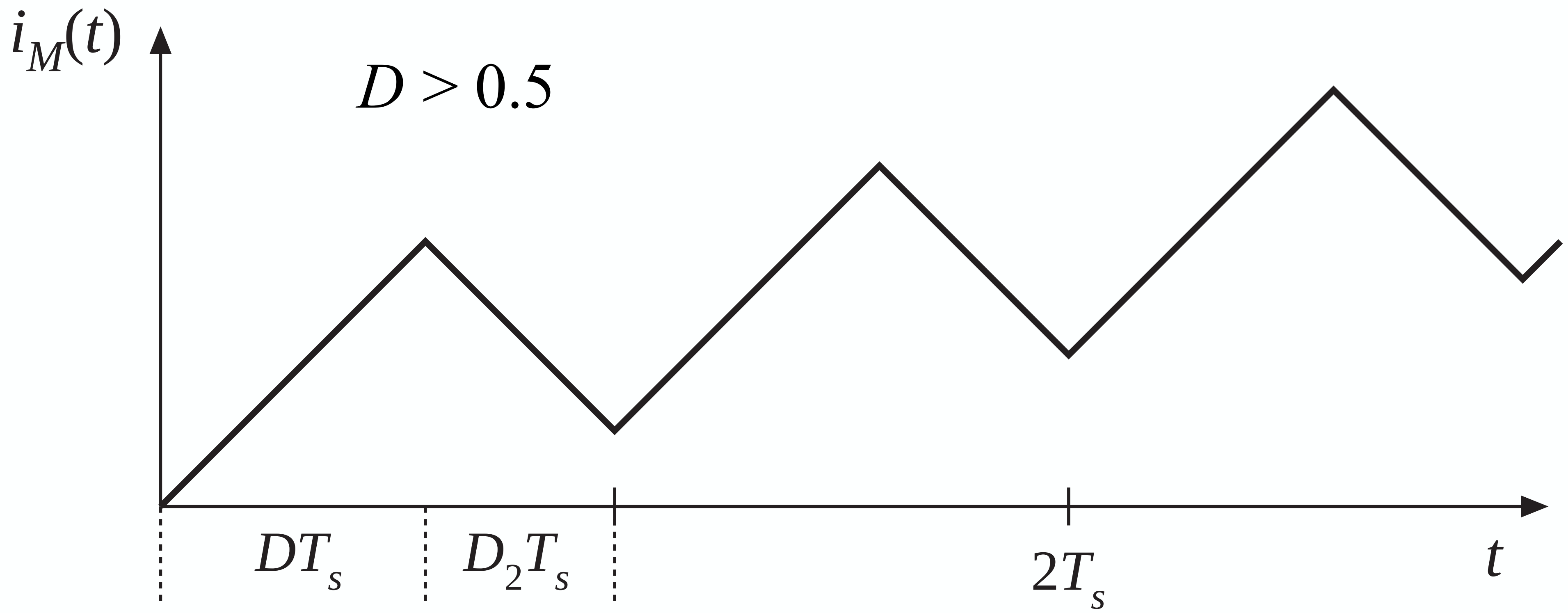
$$D \leq \frac{1}{1 + \frac{n_2}{n_1}}$$

for $n_1 = n_2$: $D \leq \frac{1}{2}$

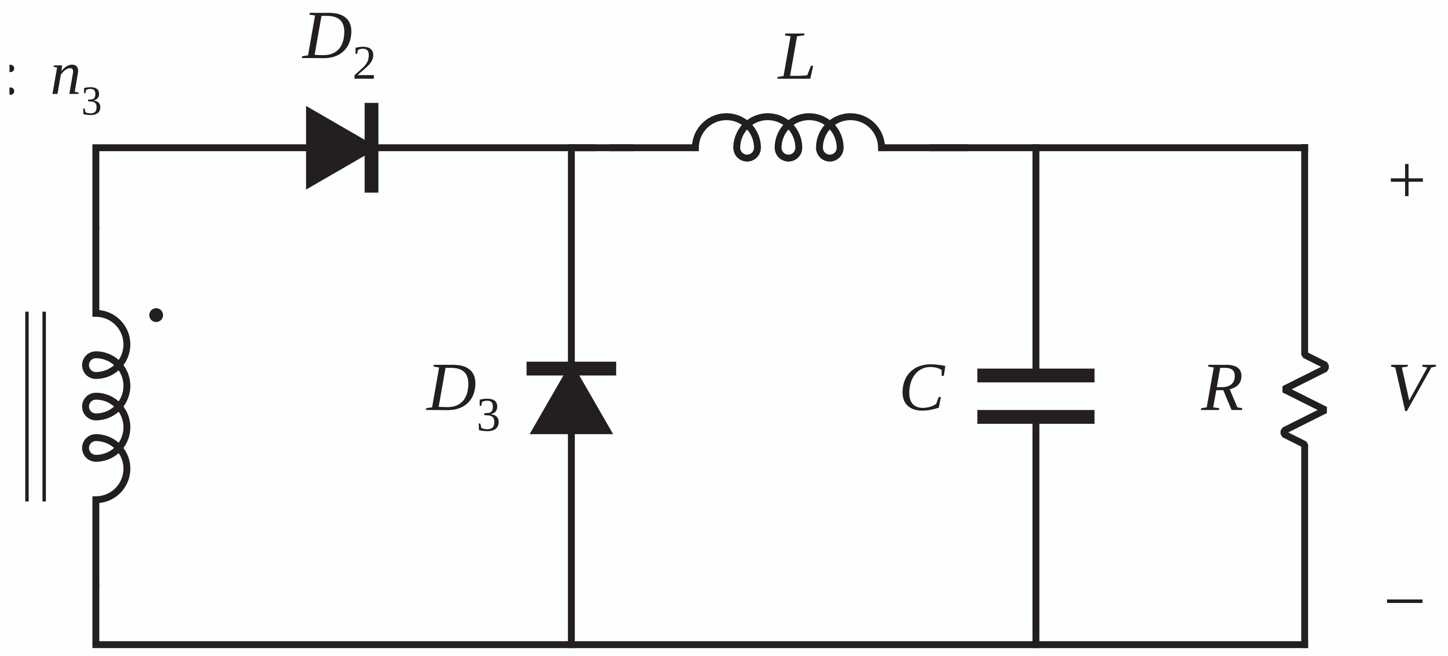
What happens when D > 0.5

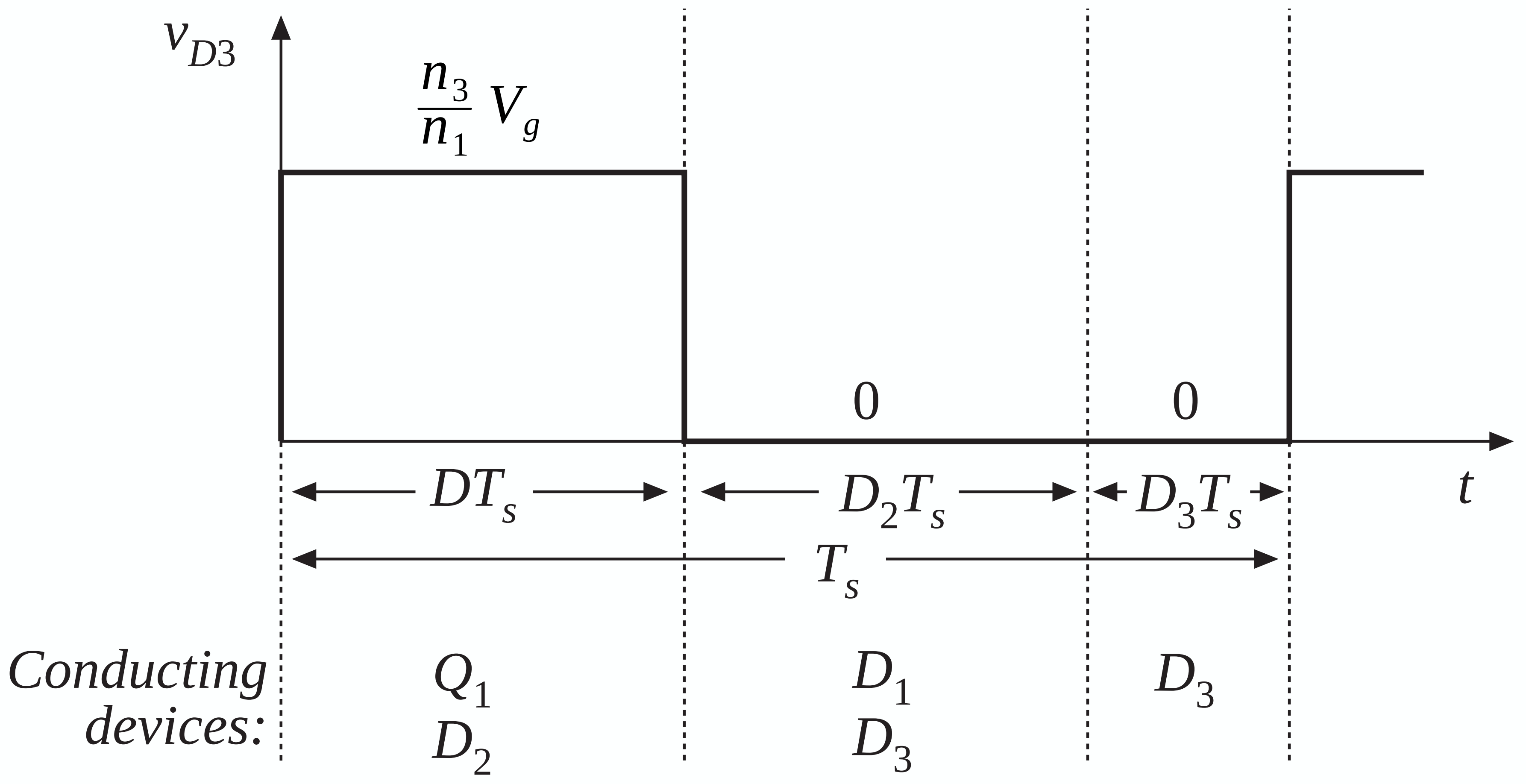
magnetizing current waveforms, for $n_1 = n_2$





Conversion ratio $M(D)$





$$\left\langle v_{D3} \right\rangle = V = \frac{n_3}{n_1} D V_g$$

Maximum duty cycle vs. transistor voltage stress

Maximum duty cycle limited to

$$D \le \frac{1}{1 + \frac{n_2}{n_1}}$$

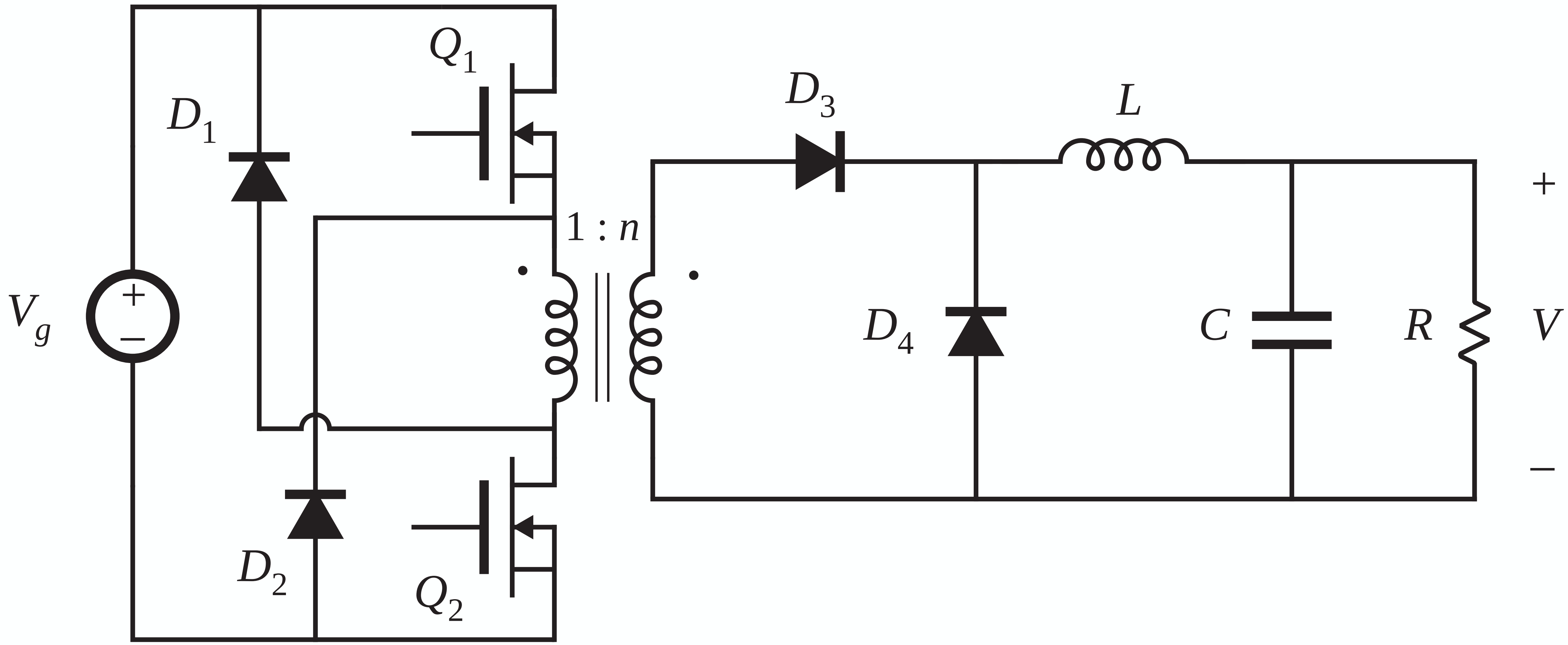
which can be increased by increasing the turns ratio n_2 / n_1. But this increases the peak transistor voltage:

$$\max\left(v_{Q1}\right) = V_g \left(1 + \frac{n_1}{n_2}\right)$$

For $n_1 = n_2$

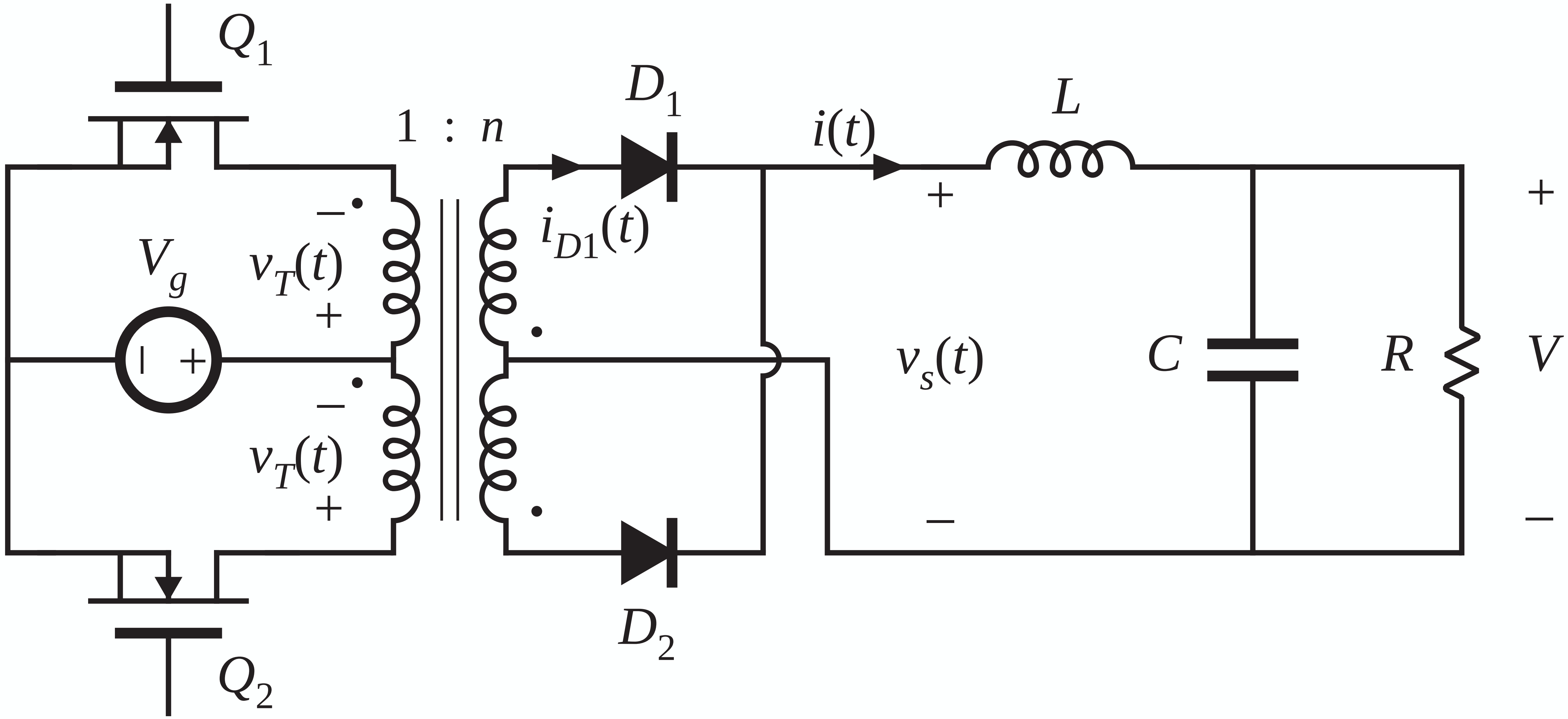
$$D \le \frac{1}{2} \qquad \text{and} \qquad \max(v_{Q1}) = 2V_g$$

The two-transistor forward converter



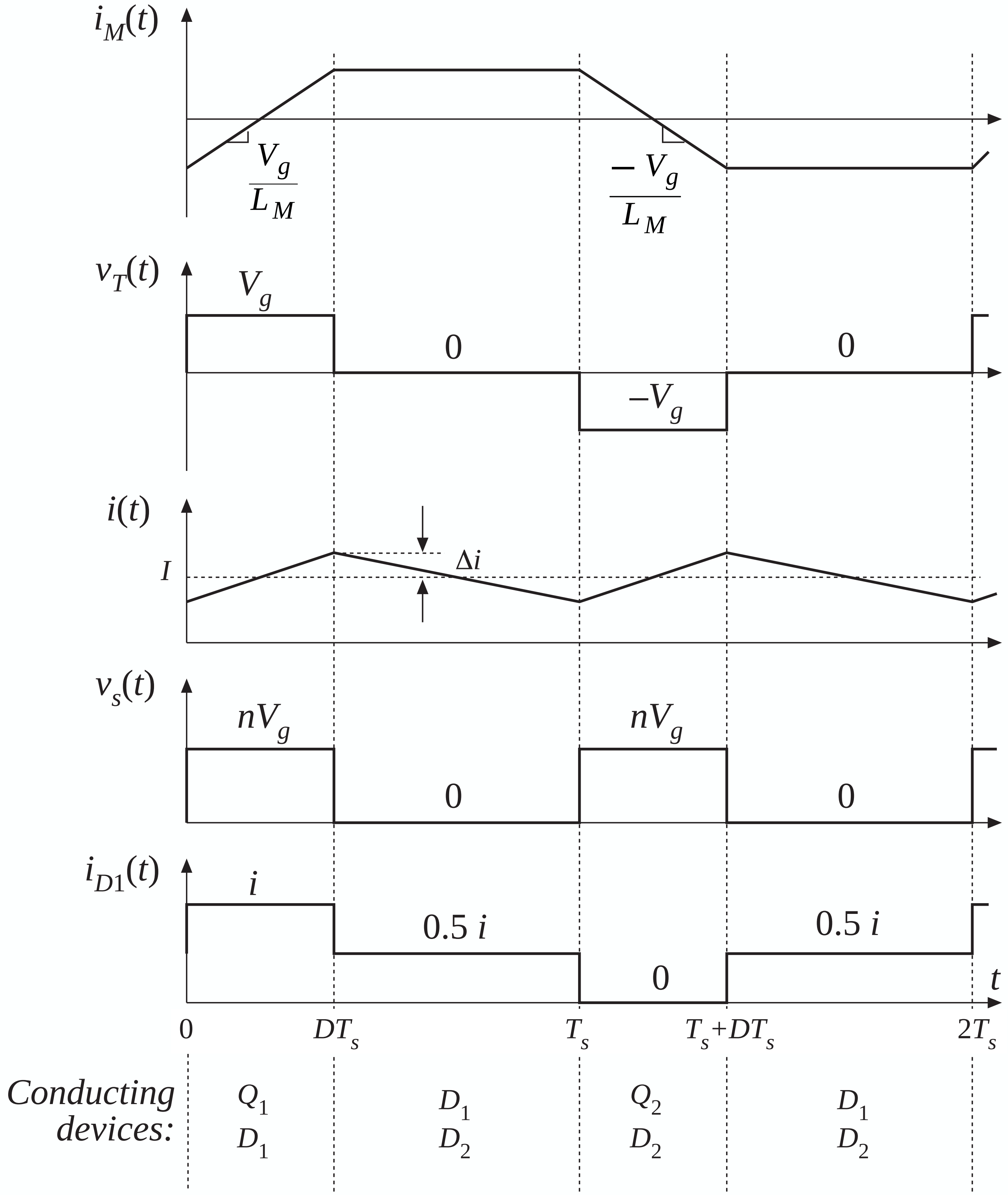
$$V = nDV_g \qquad D \le \frac{1}{2} \qquad \max(v_{Q1}) = \max(v_{Q2}) = V_g$$

6.3.3. Push-pull isolated buck converter



$V = nDV_g$ $\qquad$ $0 \leq D \leq 1$

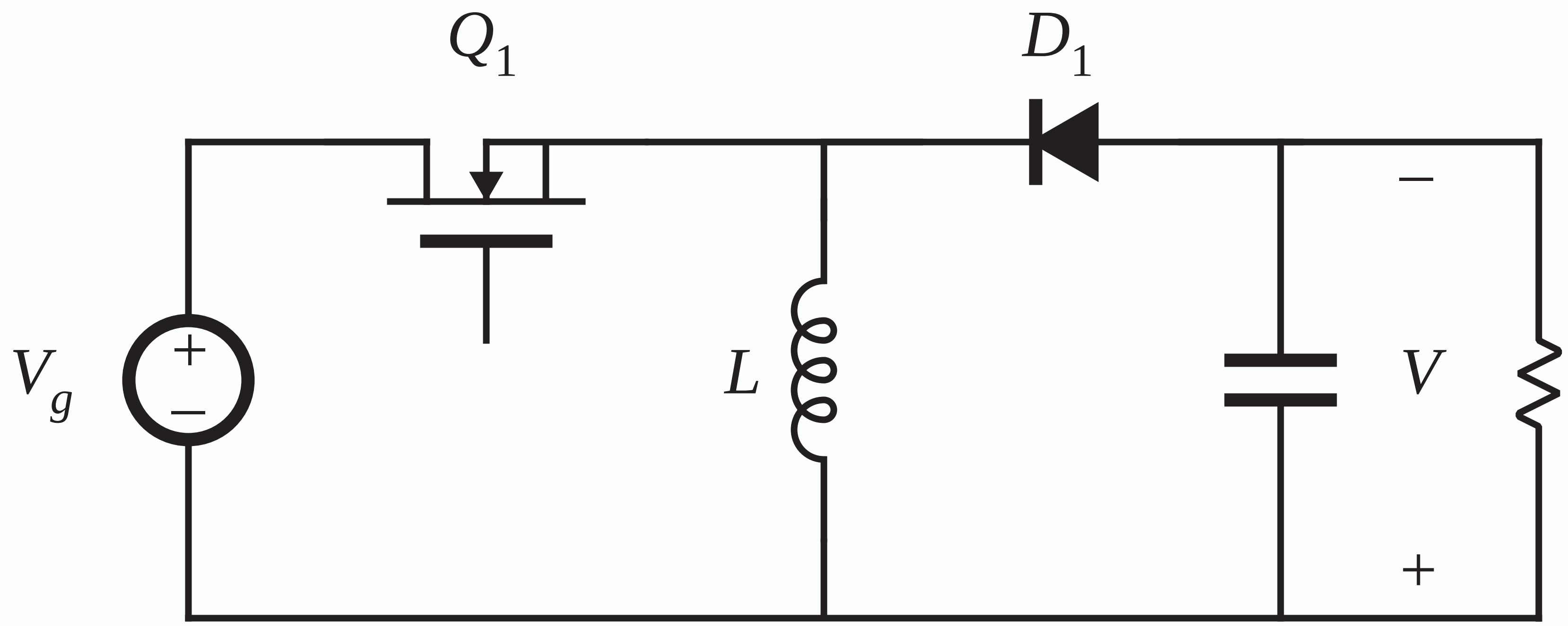
Waveforms: push-pull



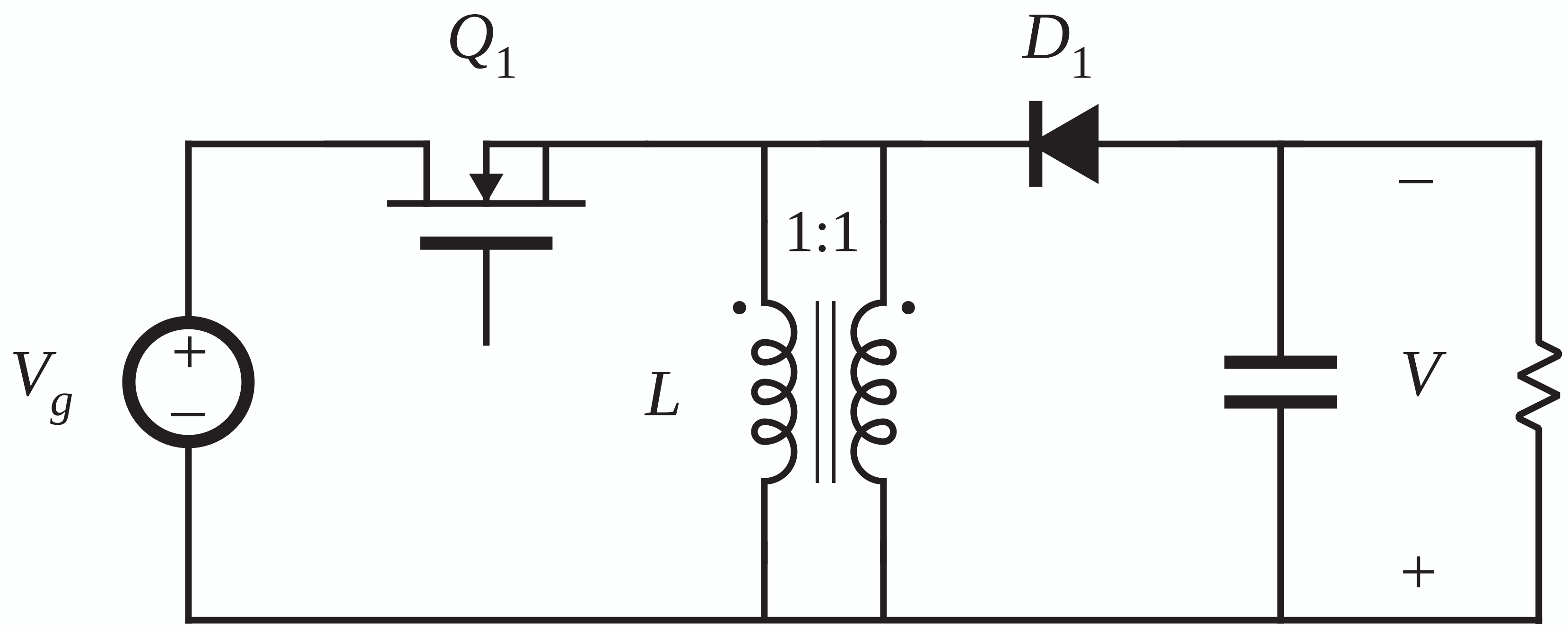
- Used with low-voltage inputs
- Secondary-side circuit identical to full bridge
- As in full bridge, transformer volt-second balance is obtained over two switching periods
- Effect of nonidealities on transformer volt-second balance?
- Current programmed control can be used to mitigate transformer saturation problems. Duty cycle control not recommended.

6.3.4. Flyback converter

buck-boost converter:

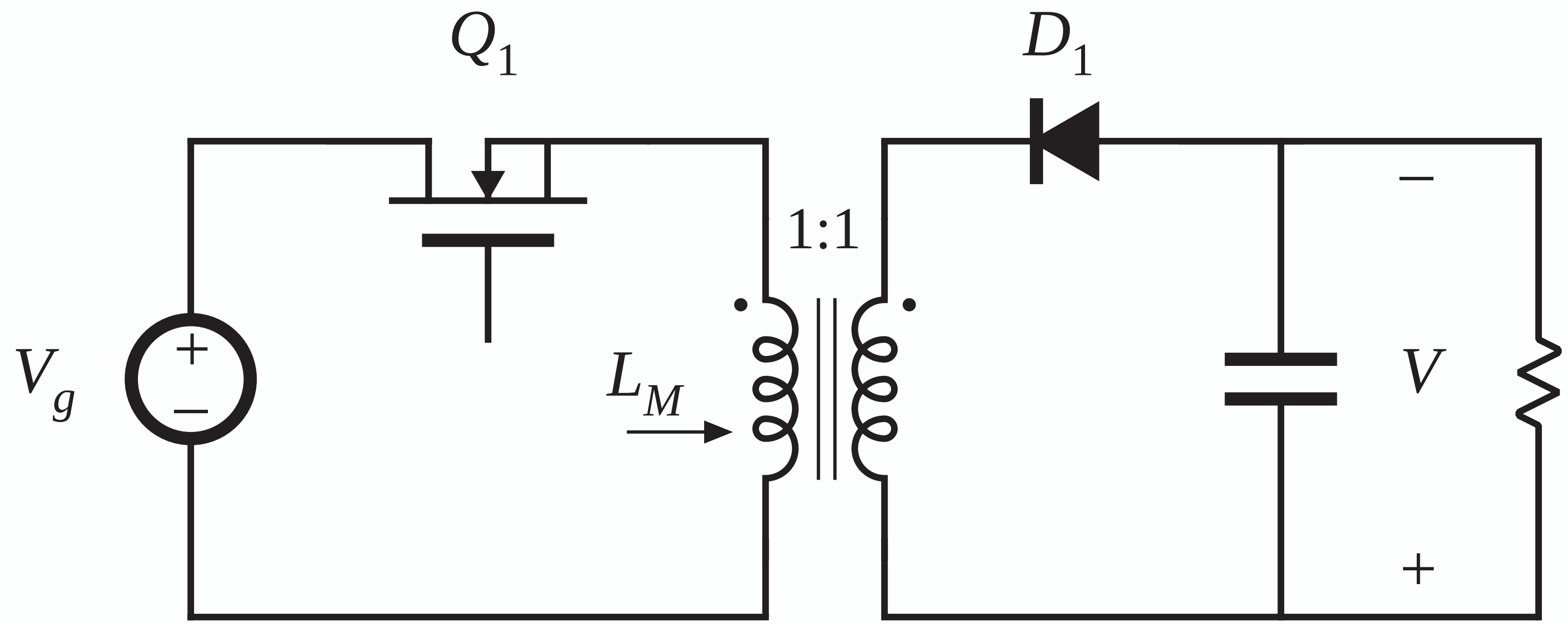


construct inductor winding using two parallel wires:

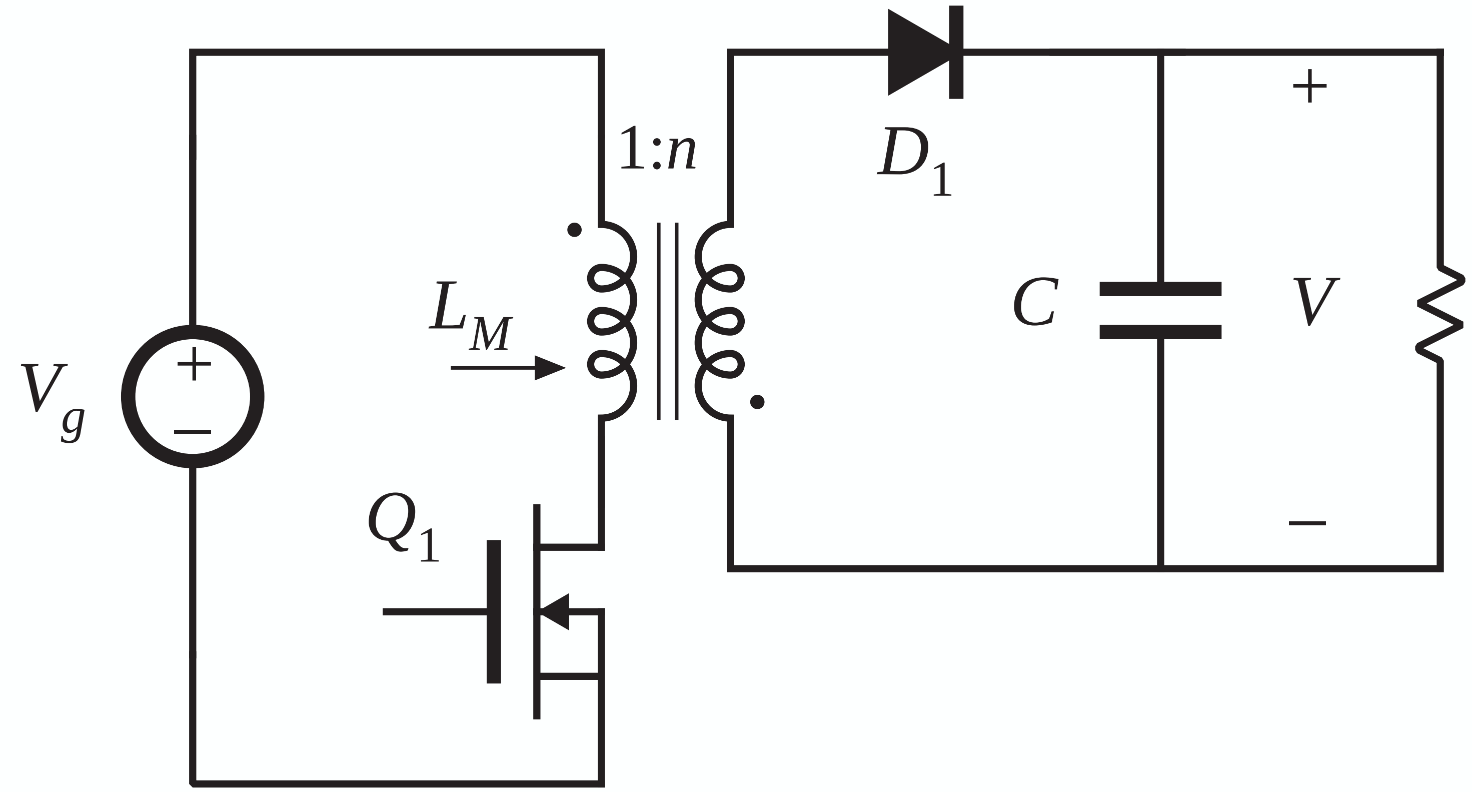


Derivation of flyback converter, cont.

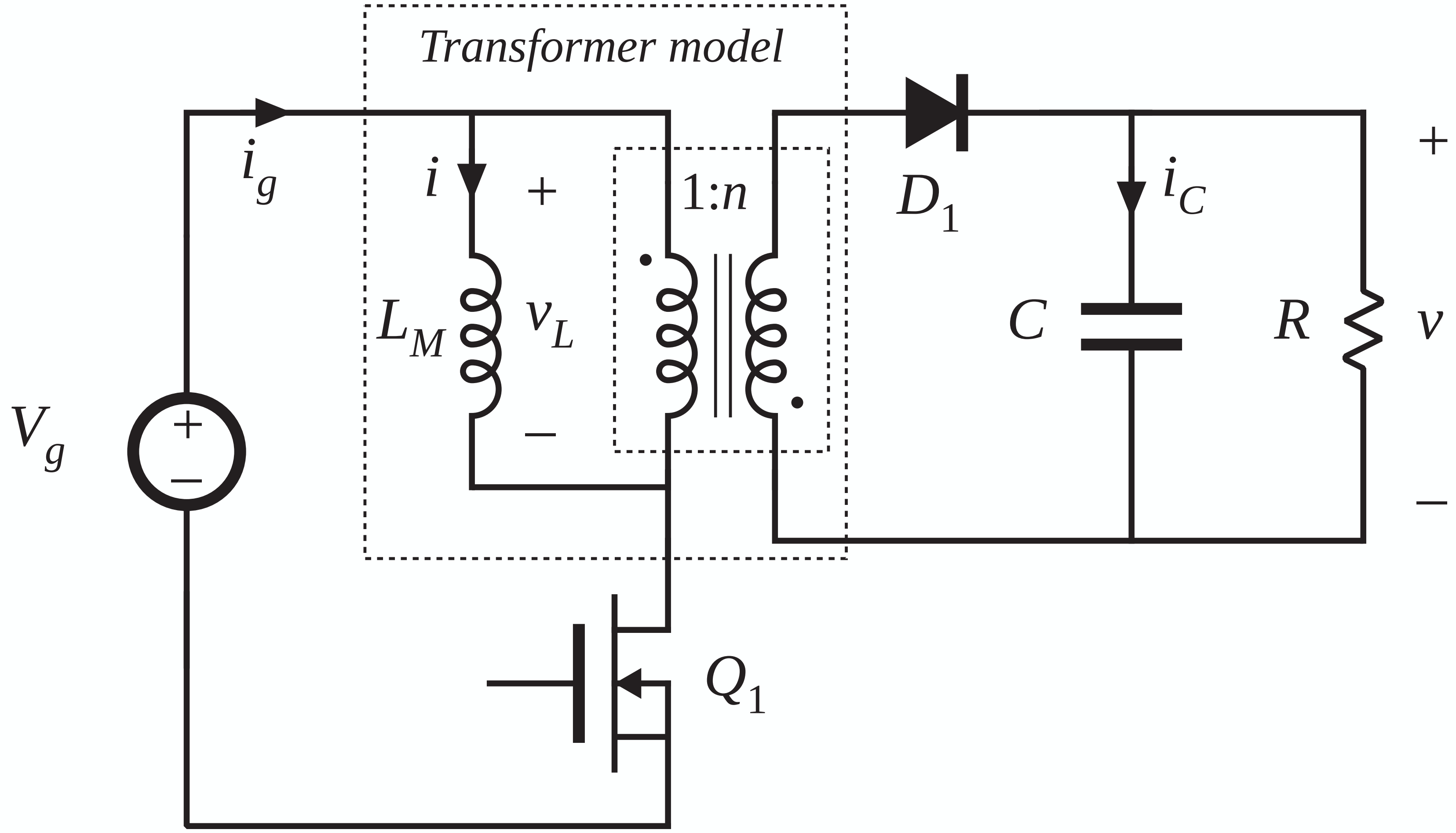
Isolate inductor windings: the flyback converter



Flyback converter having a $1{:}n$ *turns ratio and positive output:*



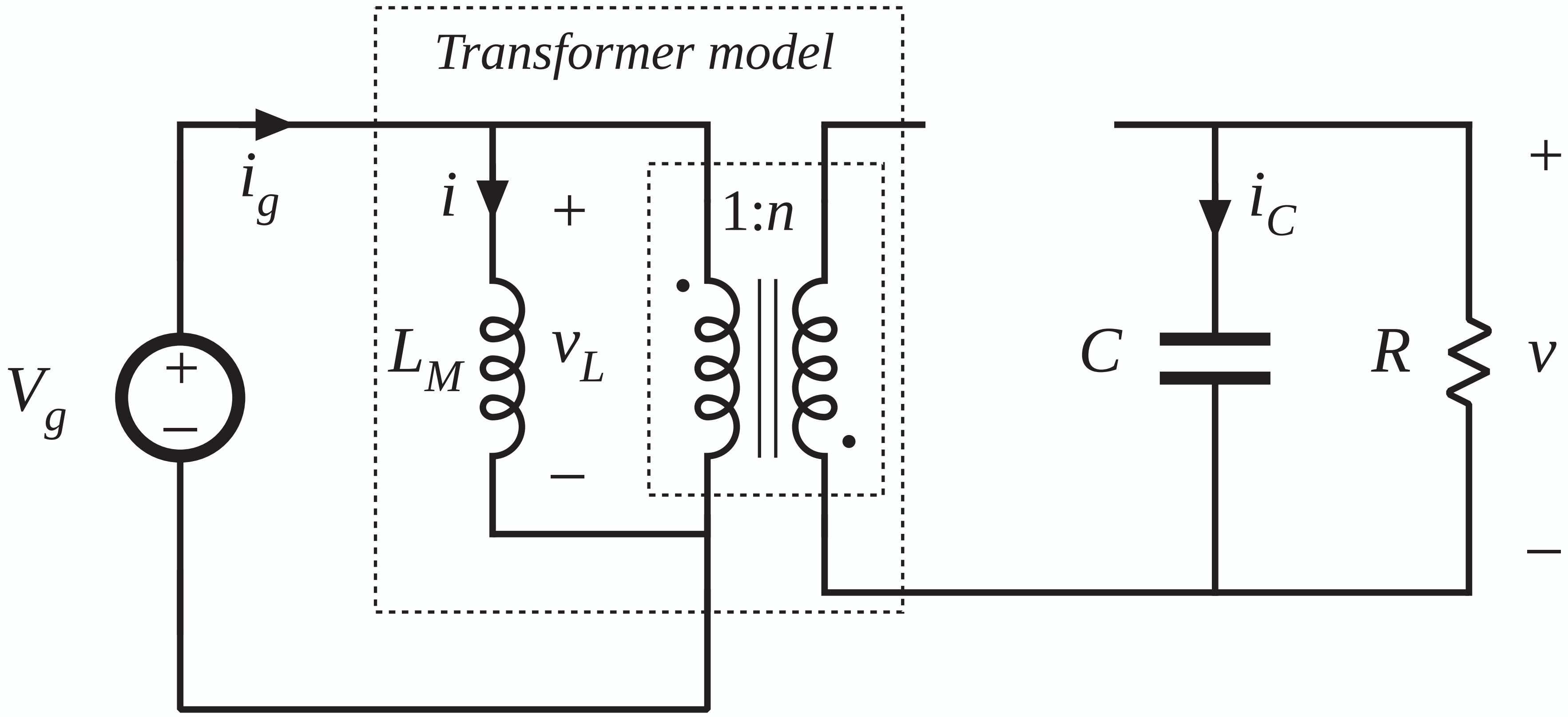
The “flyback transformer”



- A two-winding inductor
- Symbol is same as transformer, but function differs significantly from ideal transformer
- Energy is stored in magnetizing inductance
- Magnetizing inductance is relatively small

- Current does not simultaneously flow in primary and secondary windings
- Instantaneous winding voltages follow turns ratio
- Instantaneous (and rms) winding currents do not follow turns ratio
- Model as (small) magnetizing inductance in parallel with ideal transformer

Subinterval 1



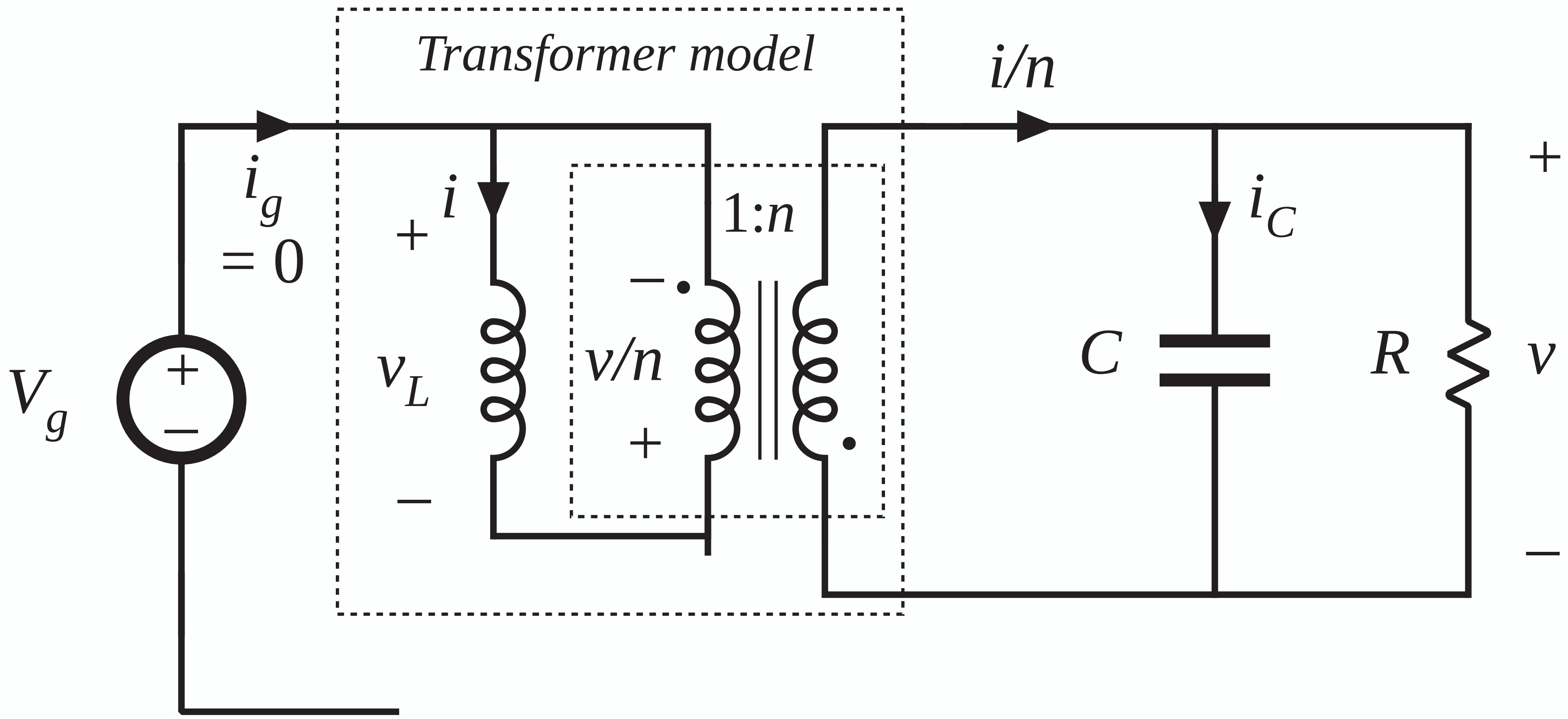
Q_1 on, D_1 off

$$v_L = V_g$$
$$i_C = -\frac{v}{R}$$
$$i_g = i$$

CCM: small ripple approximation leads to

$$v_L = V_g$$
$$i_C = -\frac{V}{R}$$
$$i_g = I$$

Subinterval 2



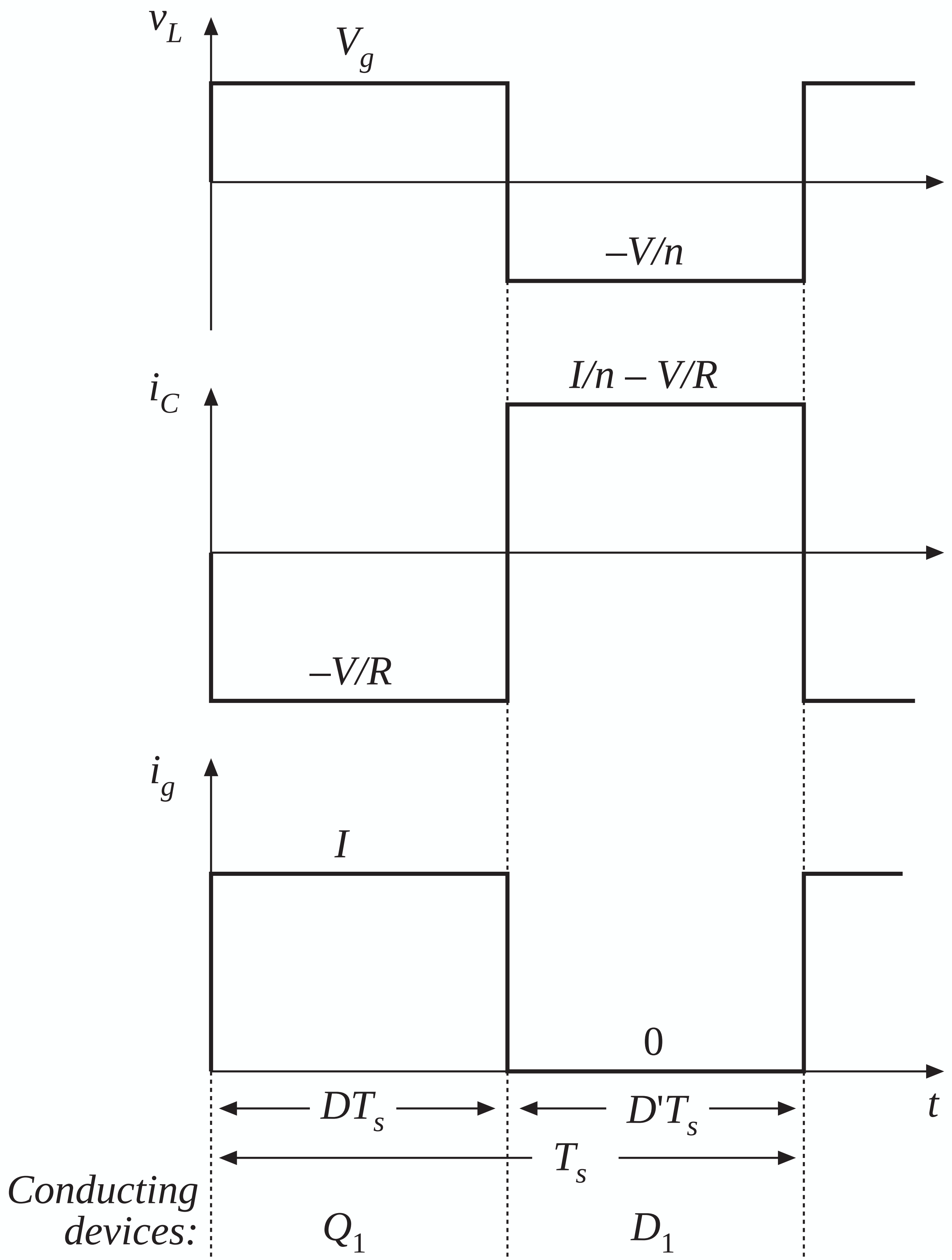
Q_1 off, D_1 on

$$v_L = -\frac{v}{n}$$
$$i_C = \frac{i}{n} - \frac{v}{R}$$
$$i_g = 0$$

CCM: small ripple approximation leads to

$$v_L = -\frac{V}{n}$$
$$i_C = \frac{I}{n} - \frac{V}{R}$$
$$i_g = 0$$

CCM Flyback waveforms and solution



Volt-second balance:

$$\langle v_L \rangle = D(V_g) + D'\left(-\frac{V}{n}\right) = 0$$

Conversion ratio is

$$M(D) = \frac{V}{V_g} = n\,\frac{D}{D'}$$

Charge balance:

$$\langle i_C \rangle = D\left(-\frac{V}{R}\right) + D'\left(\frac{I}{n} - \frac{V}{R}\right) = 0$$

Dc component of magnetizing current is

$$I = \frac{nV}{D'R}$$

Dc component of source current is

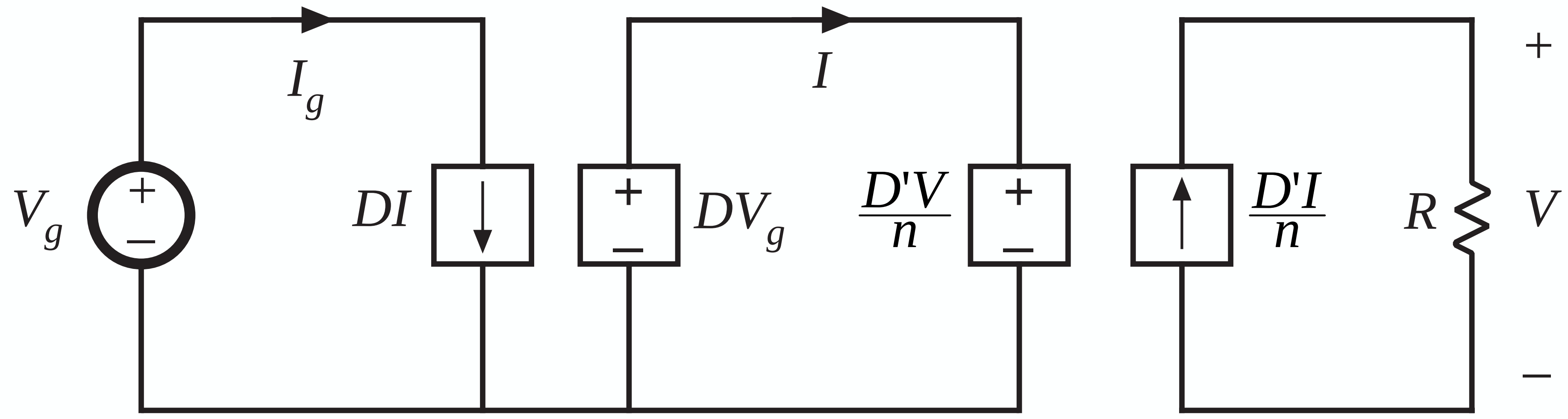
$$I_g = \langle i_g \rangle = D(I) + D'(0)$$

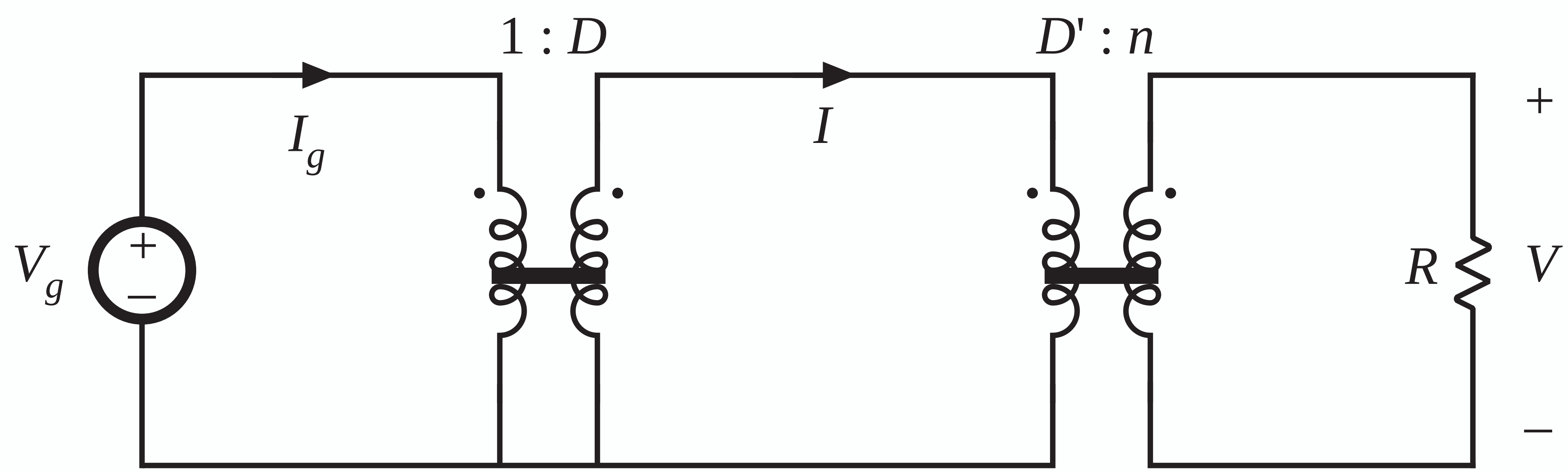
Equivalent circuit model: CCM Flyback

$$\langle v_L \rangle = D\left(V_g\right) + D'\left(-\frac{V}{n}\right) = 0$$

$$\langle i_C \rangle = D\left(-\frac{V}{R}\right) + D'\left(\frac{I}{n} - \frac{V}{R}\right) = 0$$

$$I_g = \langle i_g \rangle = D\left(I\right) + D'\left(0\right)$$





Discussion: Flyback converter

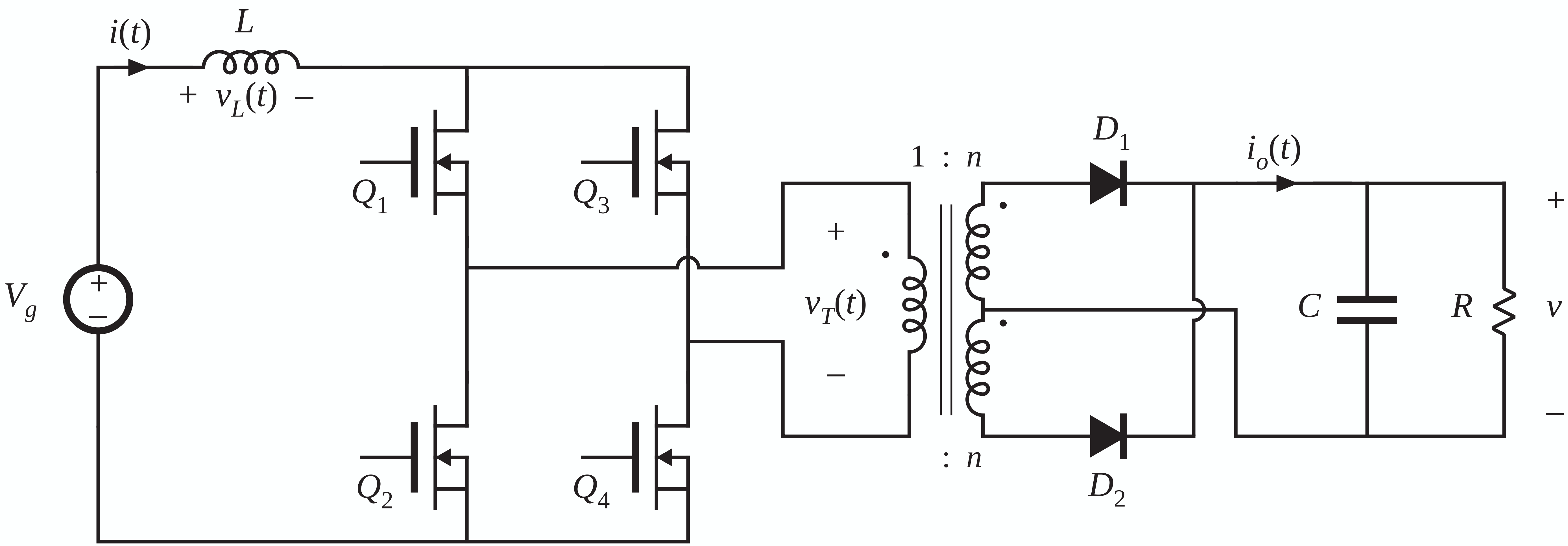
- Widely used in low power and/or high voltage applications
- Low parts count
- Multiple outputs are easily obtained, with minimum additional parts
- Cross regulation is inferior to buck-derived isolated converters
- Often operated in discontinuous conduction mode
- DCM analysis: DCM buck-boost with turns ratio

6.3.5. Boost-derived isolated converters

- A wide variety of boost-derived isolated dc-dc converters can be derived, by inversion of source and load of buck-derived isolated converters:
  - full-bridge and half-bridge isolated boost converters
  - inverse of forward converter: the “reverse” converter
  - push-pull boost-derived converter

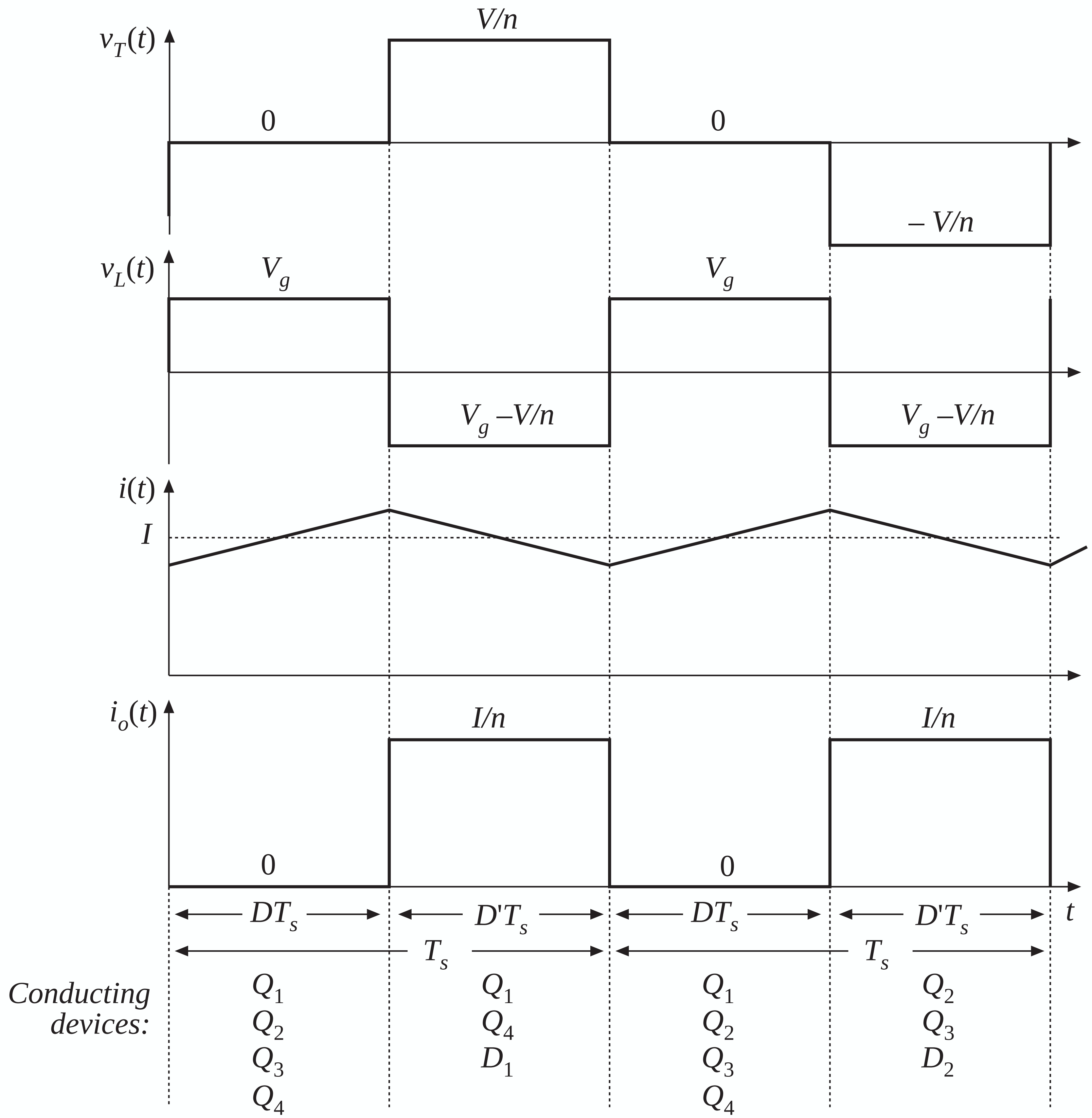
Of these, the full-bridge and push-pull boost-derived isolated converters are the most popular, and are briefly discussed here.

Full-bridge transformer-isolated boost-derived converter



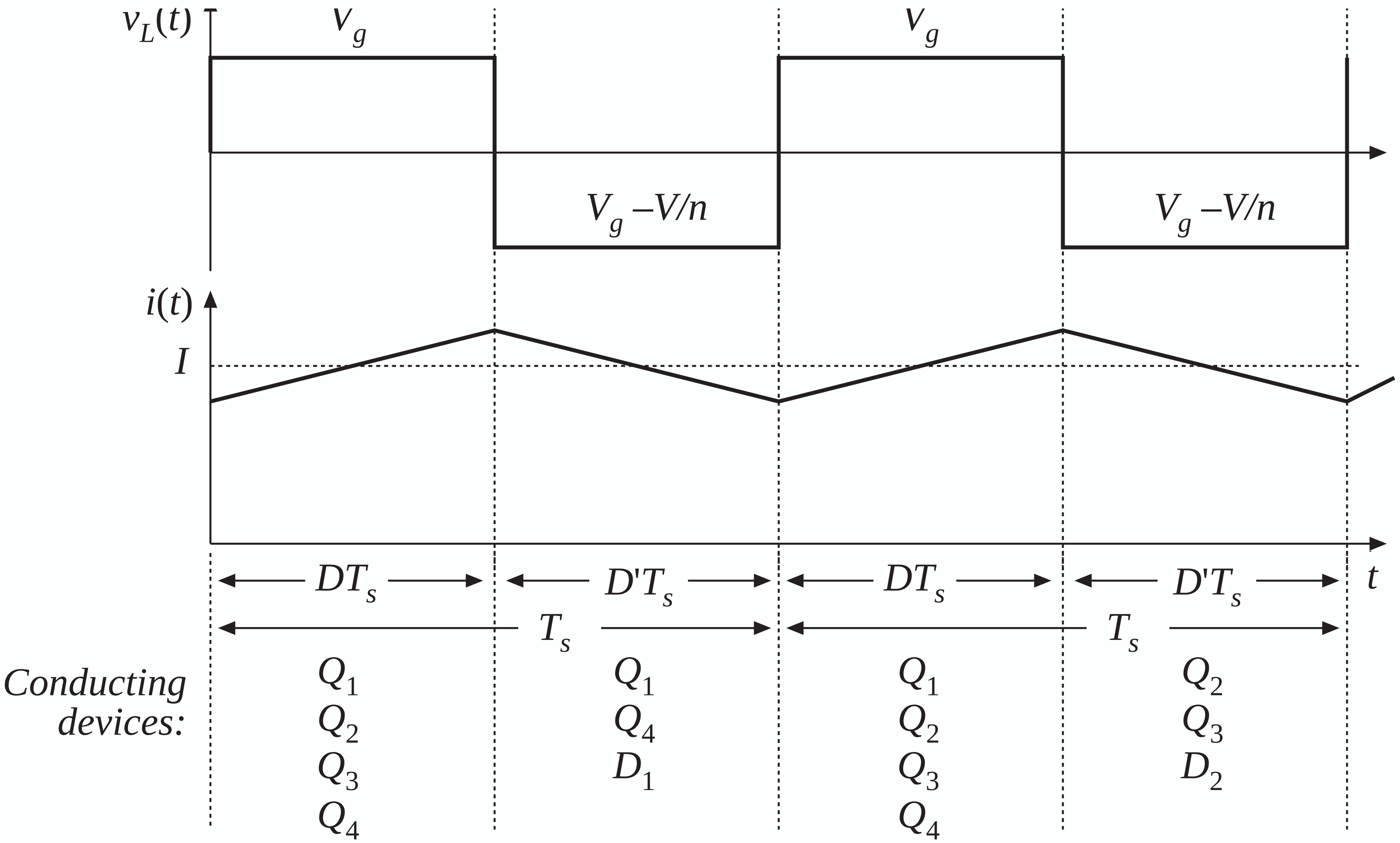
- Circuit topologies are equivalent to those of nonisolated boost converter
- With 1:1 turns ratio, inductor current $i(t)$ and output current $i_o(t)$ waveforms are identical to nonisolated boost converter

Transformer reset mechanism



- As in full-bridge buck topology, transformer volt-second balance is obtained over two switching periods.
- During first switching period: transistors Q_1 and Q_4 conduct for time DT_s , applying volt-seconds VDT_s to secondary winding.
- During next switching period: transistors Q_2 and Q_3 conduct for time DT_s , applying volt-seconds $-VDT_s$ to secondary winding.

Conversion ratio $M(D)$



Application of volt-second balance to inductor voltage waveform:

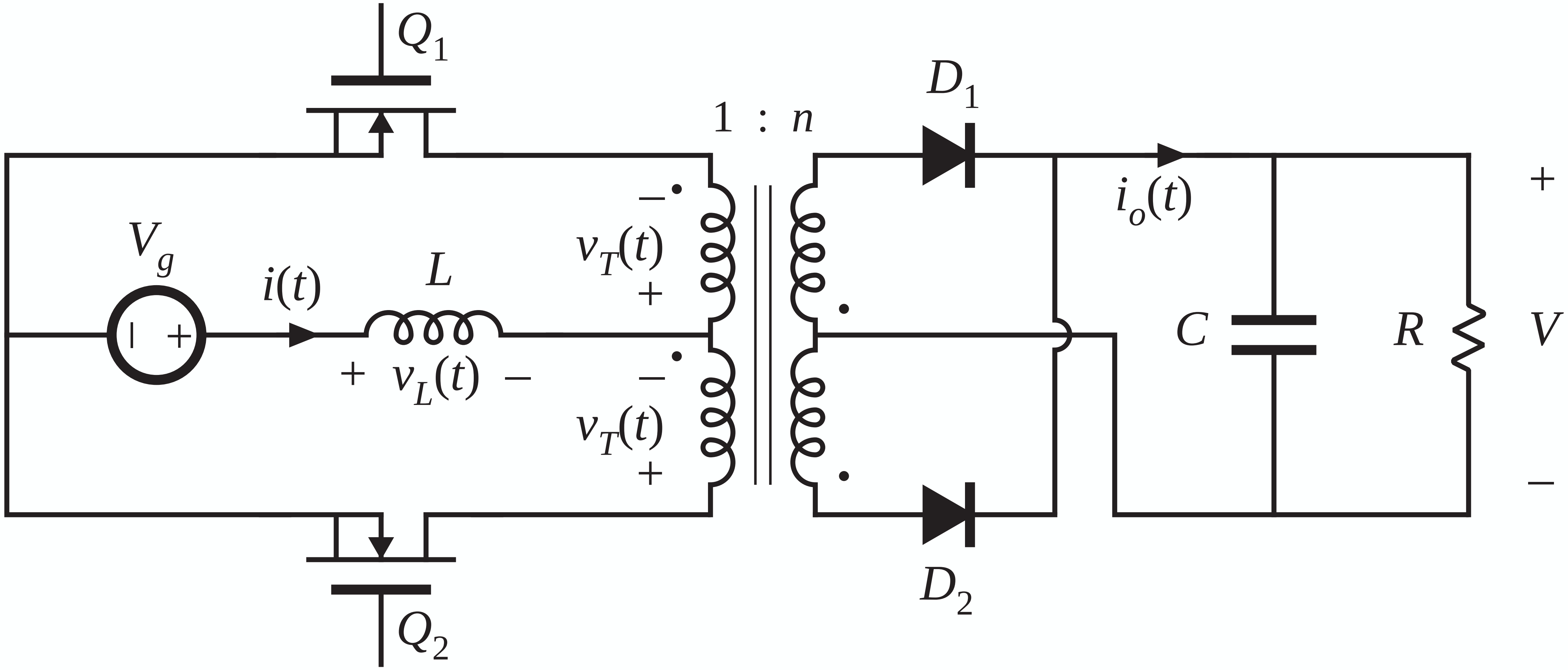
$$\left\langle v_L \right\rangle = D\left(V_g\right) + D'\left(V_g - \frac{V}{n}\right) = 0$$

Solve for $M(D)$:

$$M(D) = \frac{V}{V_g} = \frac{n}{D'}$$

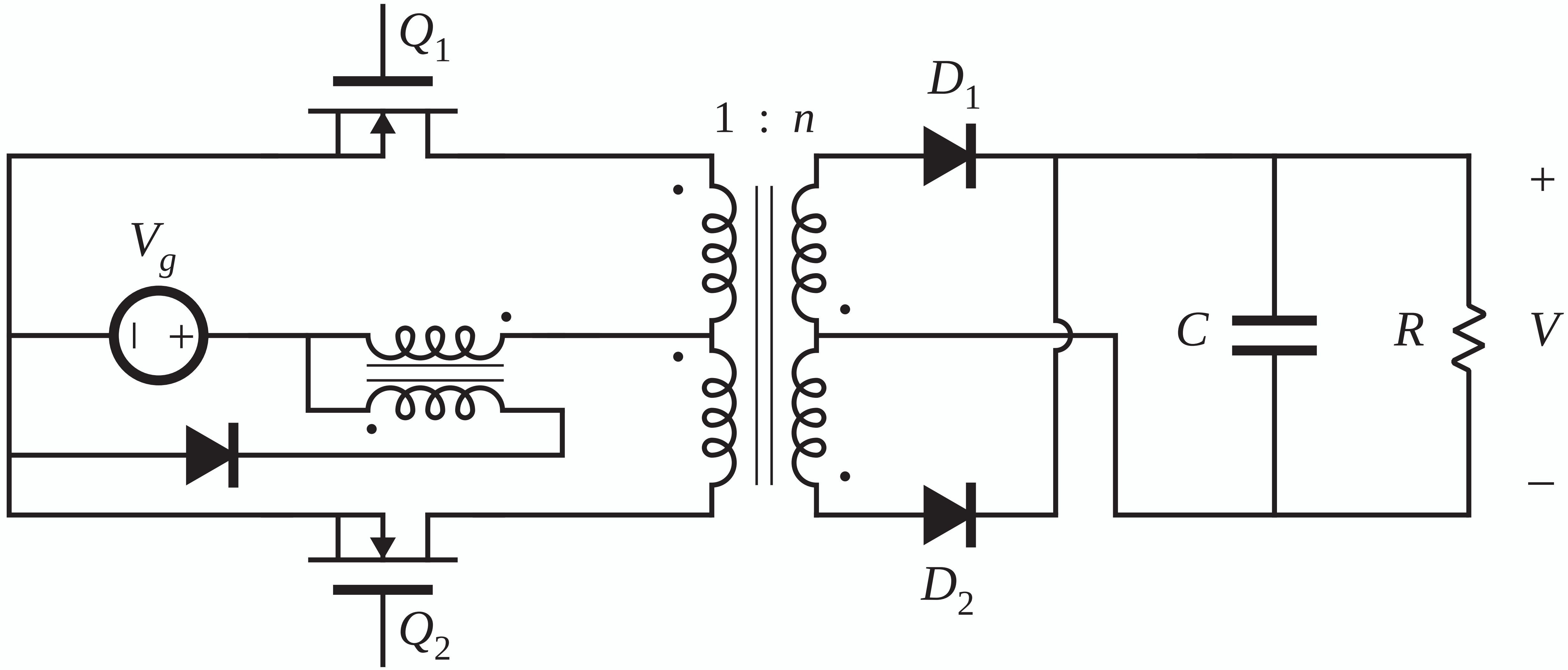
—boost with turns ratio n

Push-pull boost-derived converter



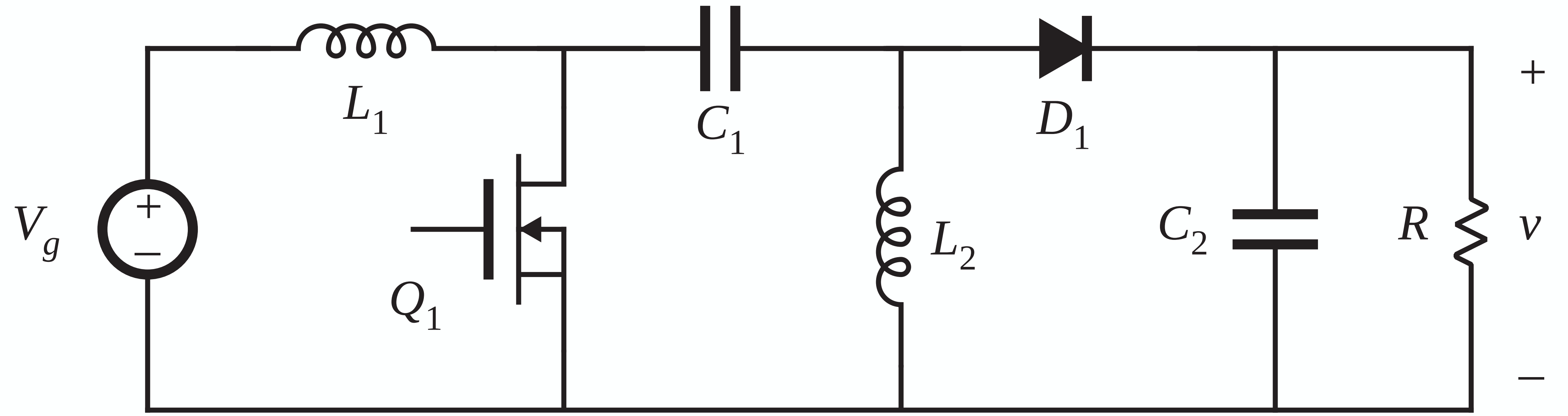
$$M(D) = \frac{V}{V_g} = \frac{n}{D'}$$

Push-pull converter based on Watkins-Johnson converter

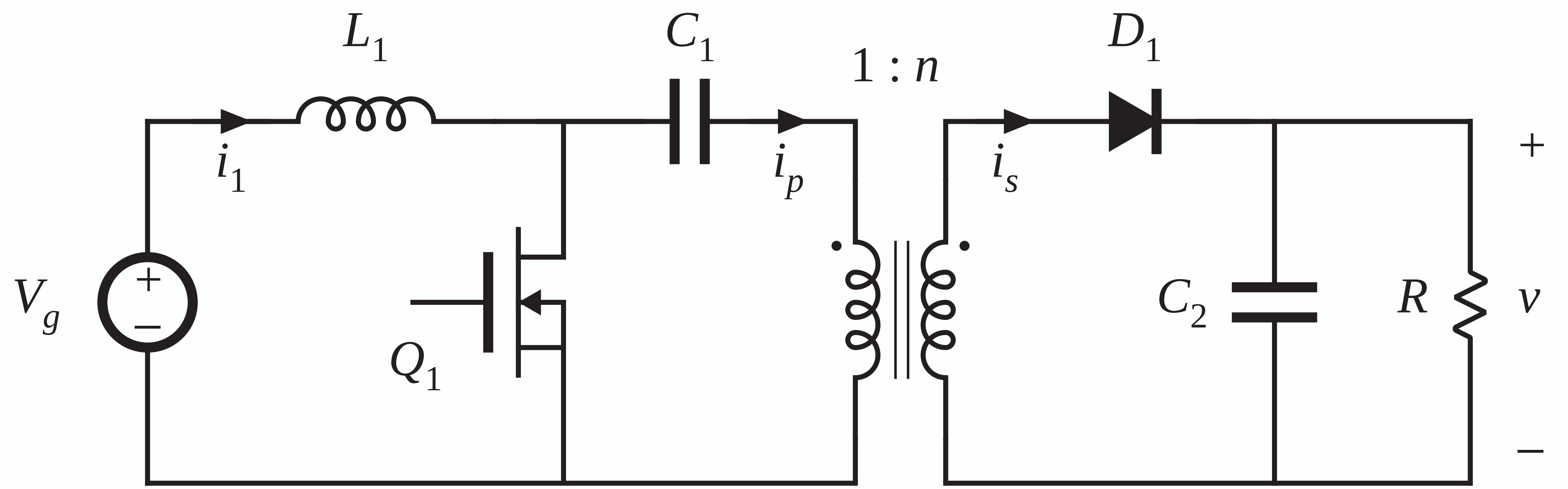


6.3.6. Isolated versions of the SEPIC and Cuk converter

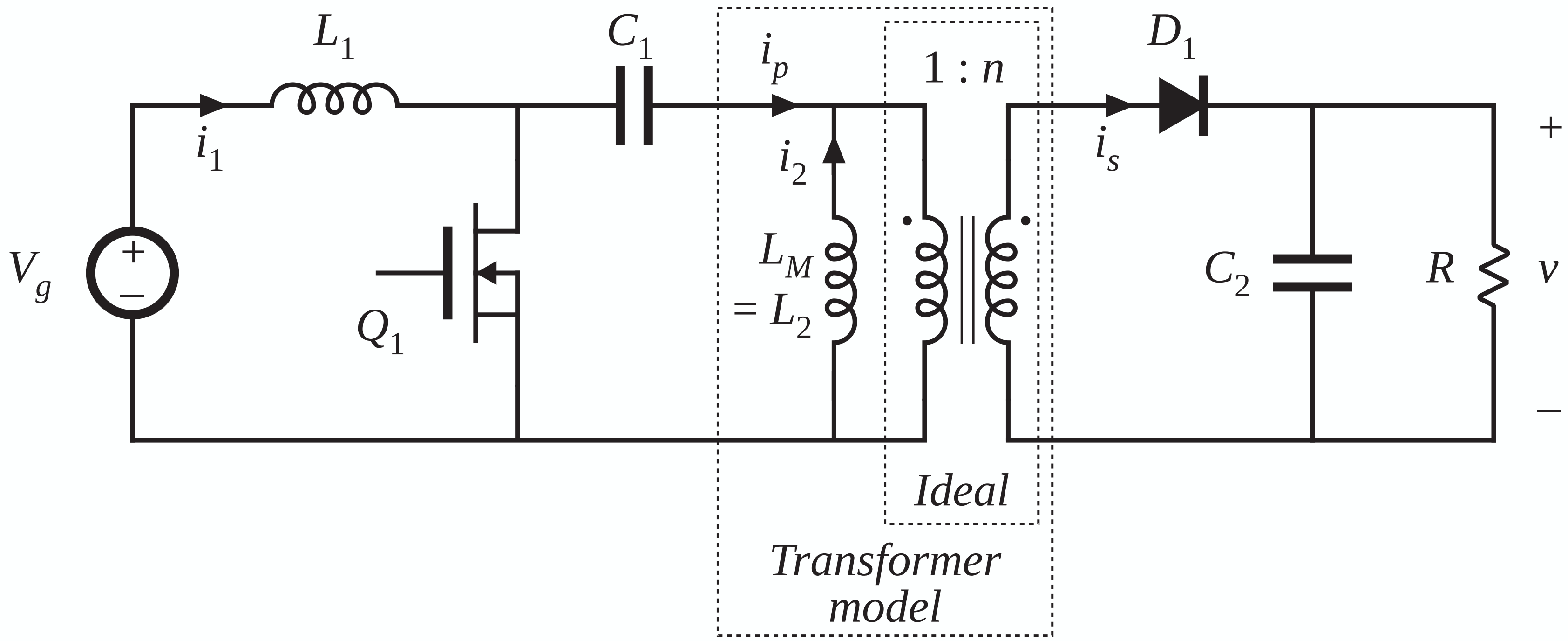
Basic nonisolated SEPIC



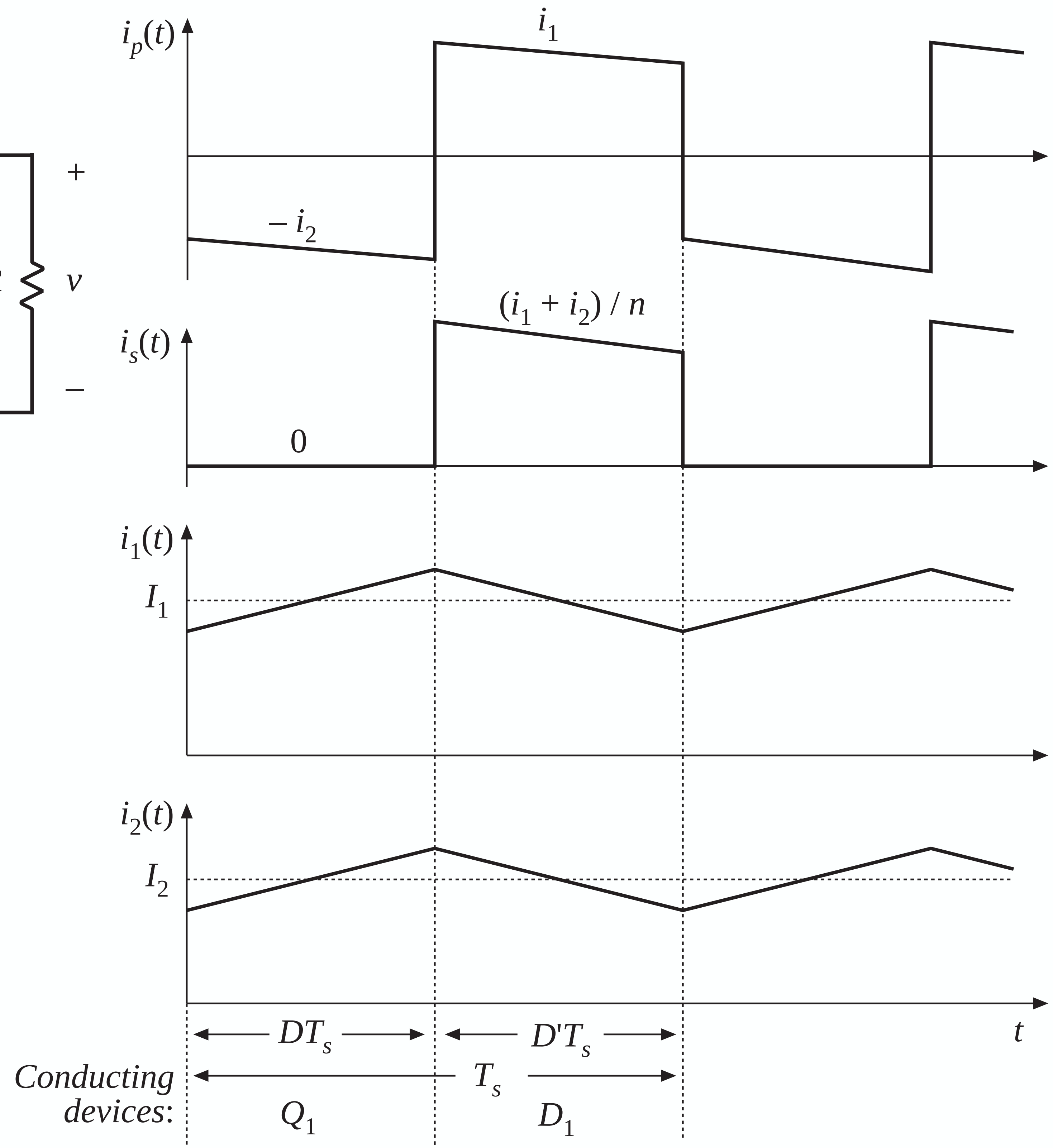
Isolated SEPIC



Isolated SEPIC

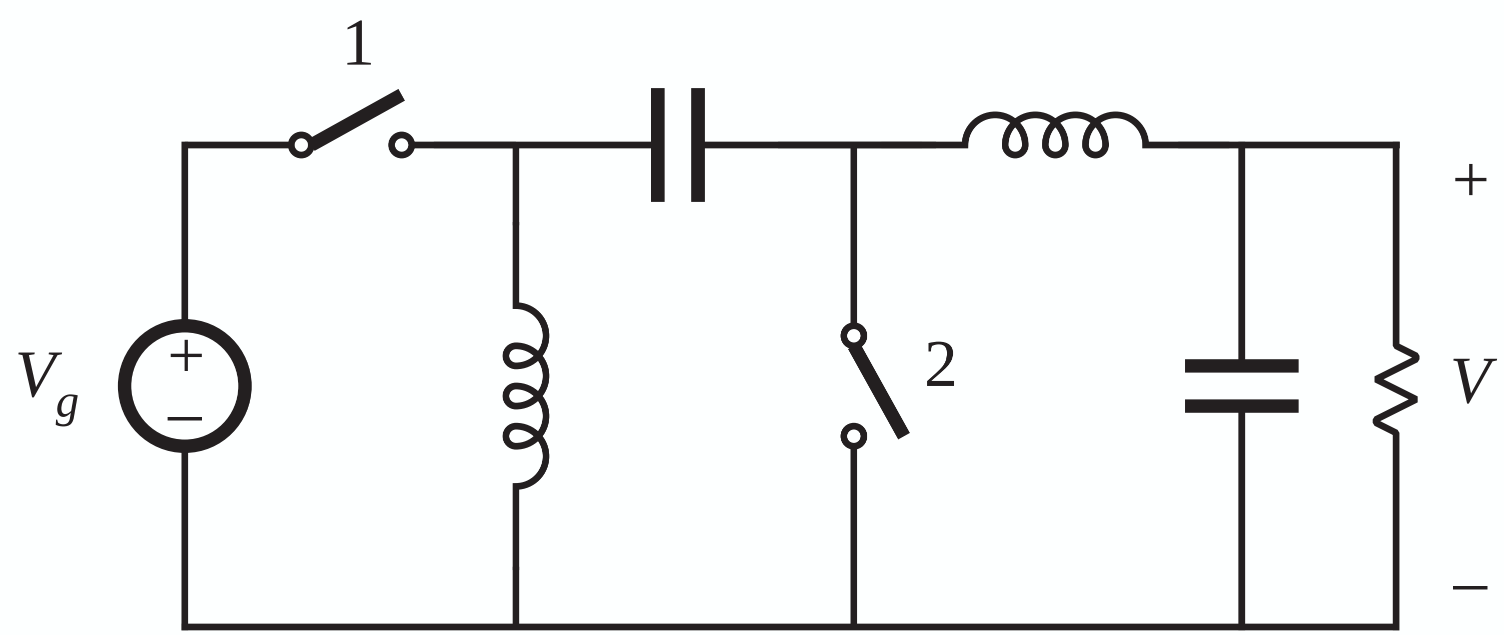


$$M(D) = \frac{V}{V_g} = \frac{nD}{D'}$$

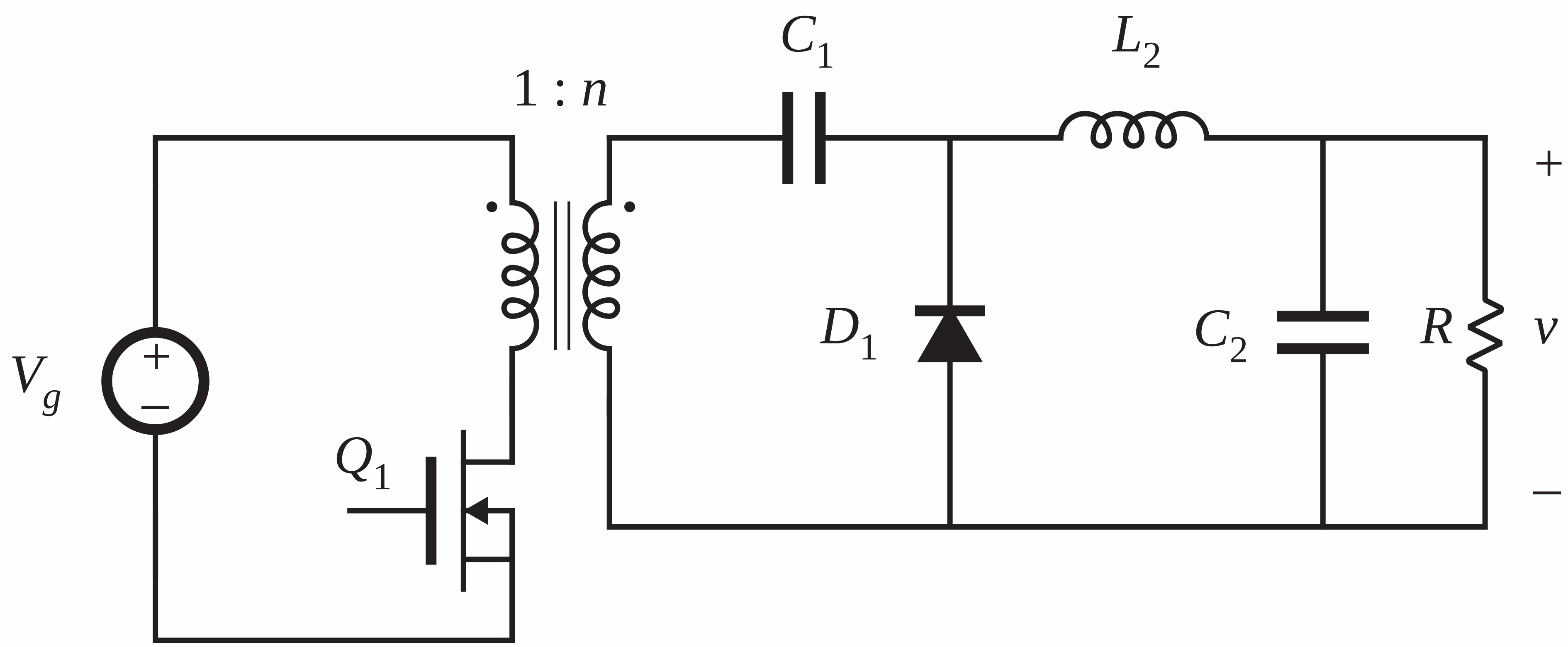


Inverse SEPIC

Nonisolated inverse SEPIC

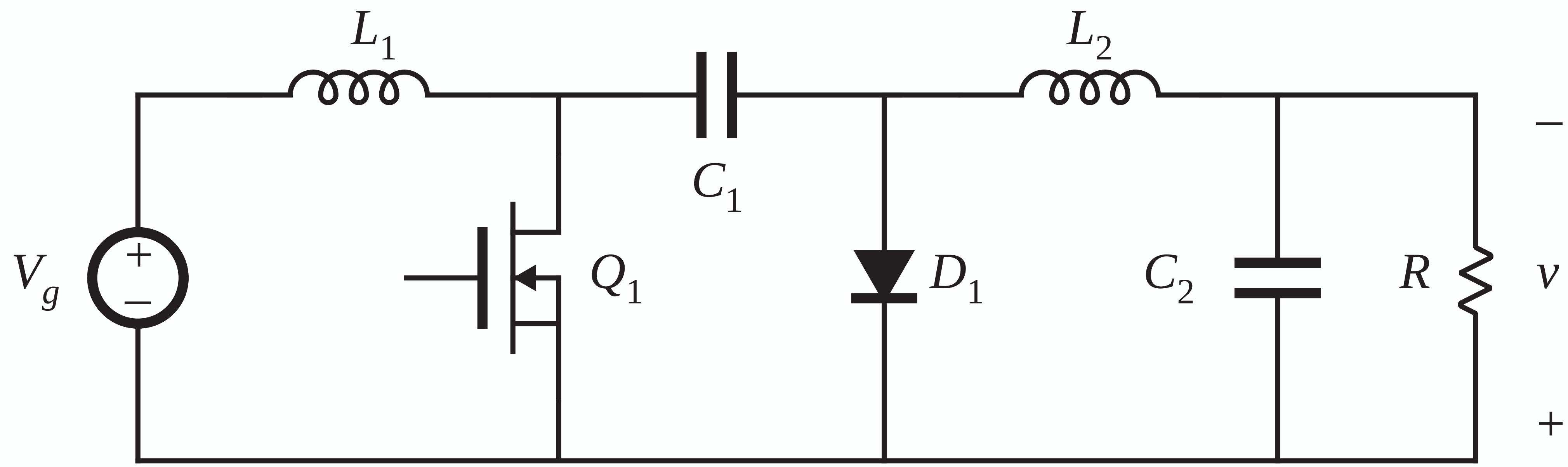


Isolated inverse SEPIC

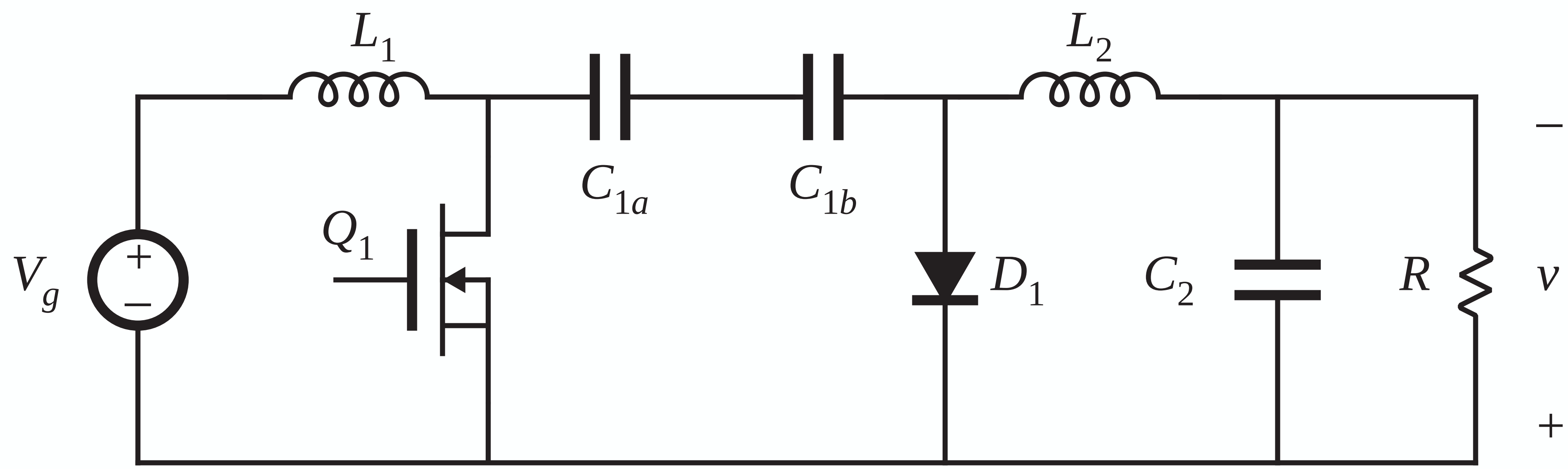


Obtaining isolation in the Cuk converter

Nonisolated Cuk converter



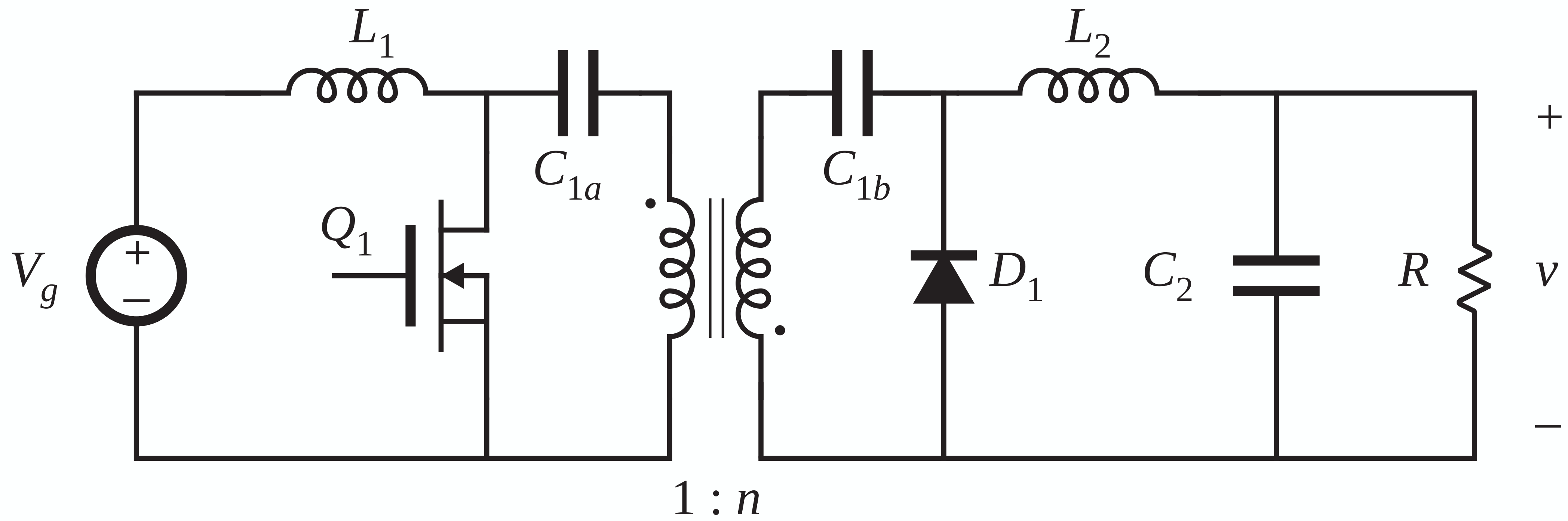
Split capacitor C_1 *into series capacitors* C_{1a} *and* C_{1b}



Isolated Cuk converter

Insert transformer between capacitors C_{1a} and C_{1b}

$$M(D) = \frac{V}{V_g} = \frac{nD}{D'}$$



Discussion

- Capacitors C_{1a} *and* C_{1b} ensure that no dc voltage is applied to transformer primary or secondary windings
- Transformer functions in conventional manner, with small magnetizing current and negligible energy storage within the magnetizing inductance

6.4. Converter evaluation and design

For a given application, which converter topology is best?

There is no ultimate converter, perfectly suited for all possible applications

Trade studies

- Rough designs of several converter topologies to meet the given specifications
- An unbiased quantitative comparison of worst-case transistor currents and voltages, transformer size, etc.

Comparison via switch stress, switch utilization, and semiconductor cost

Spreadsheet design

6.4.1. Switch stress and switch utilization

- Largest single cost in a converter is usually the cost of the active semiconductor devices
- Conduction and switching losses associated with the active semiconductor devices often dominate the other sources of loss

This suggests evaluating candidate converter approaches by comparing the voltage and current stresses imposed on the active semiconductor devices.

Minimization of total switch stresses leads to reduced loss, and to minimization of the total silicon area required to realize the power devices of the converter.

Total active switch stress S

In a converter having k active semiconductor devices, the total active switch stress S is defined as

$$S = \sum_{j=1}^{k} V_j I_j$$

where

V_j is the peak voltage applied to switch j,

I_j is the rms current applied to switch j (peak current is also sometimes used).

In a good design, the total active switch stress is minimized.

Active switch utilization U

It is desired to minimize the total active switch stress, while maximizing the output power P_{load}.

The active switch utilization U is defined as

$$U = \frac{P_{load}}{S}$$

The active switch utilization is the converter output power obtained per unit of active switch stress. It is a converter figure-of-merit, which measures how well a converter utilizes its semiconductor devices.

Active switch utilization is less than 1 in transformer-isolated converters, and is a quantity to be maximized.

Converters having low switch utilizations require extra active silicon area, and operate with relatively low efficiency.

Active switch utilization is a function of converter operating point.

CCM flyback example: Determination of S

During subinterval 2, the transistor blocks voltage $V_{Q1,pk}$ equal to V_g plus the reflected load voltage:

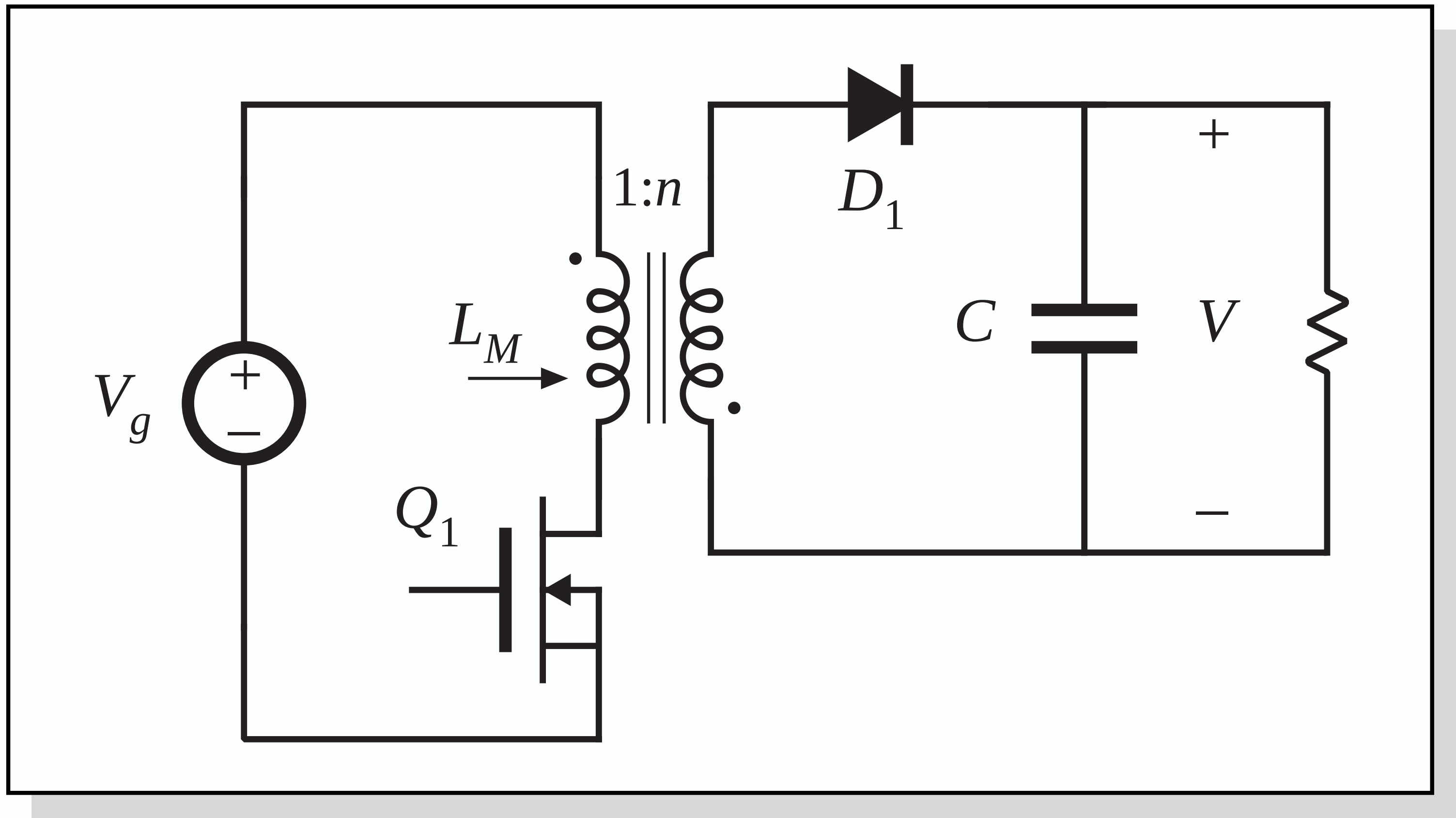
$$V_{Q1,pk} = V_g + \frac{V}{n} = \frac{V_g}{D'}$$

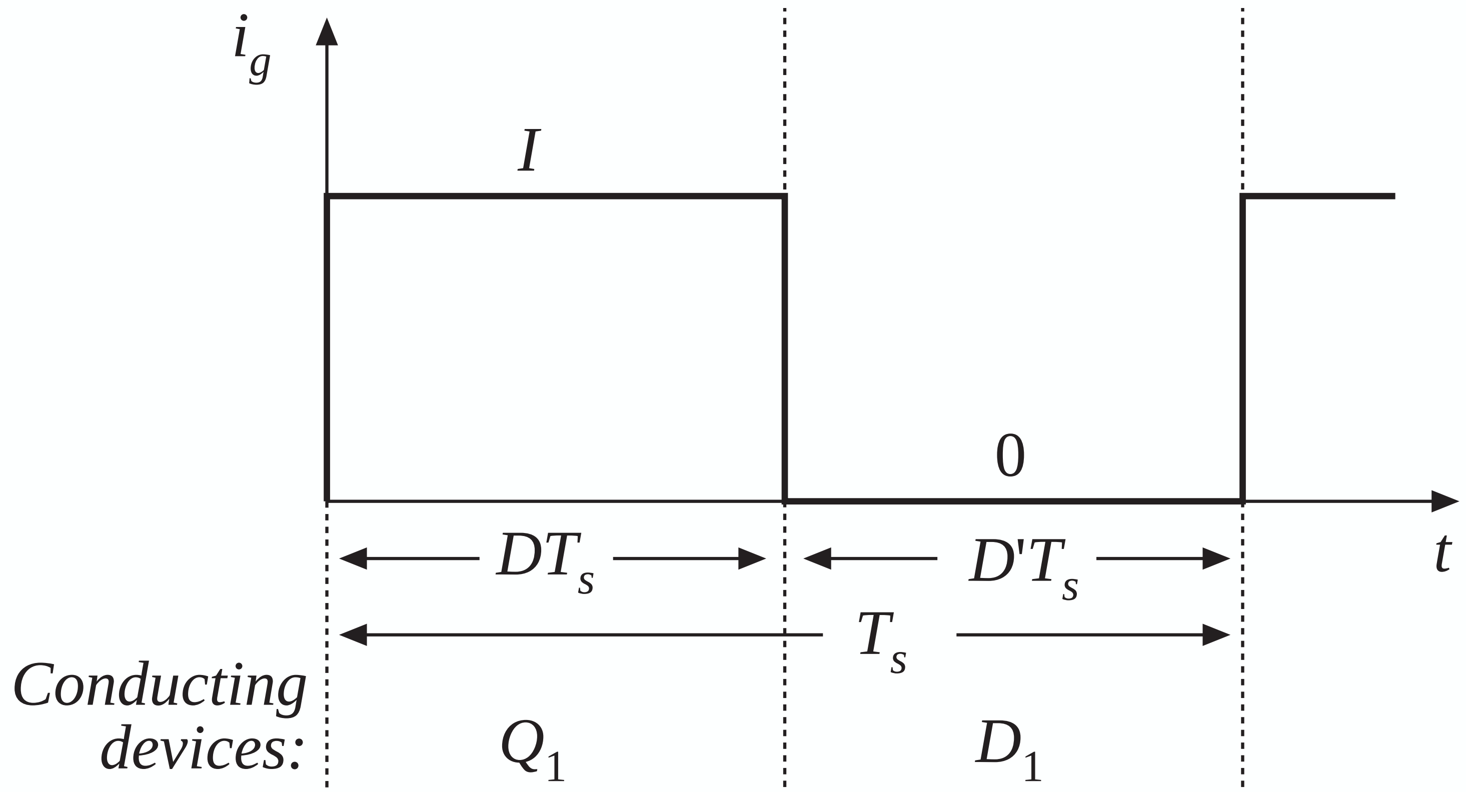
Transistor current coincides with $i_g(t)$. RMS value is

$$I_{Q1,rms} = I\sqrt{D} = \frac{P_{load}}{V_g\sqrt{D}}$$

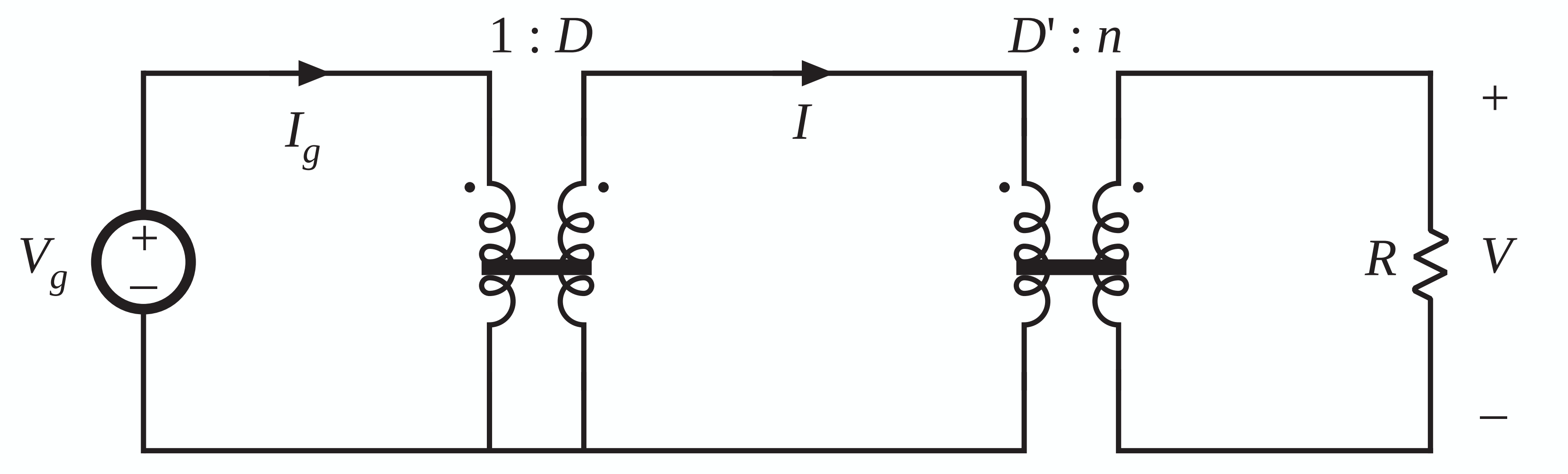
Switch stress S is

$$S = V_{Q1,pk}\, I_{Q1,rms} = \left(V_g + \frac{V}{n}\right)\left(I\sqrt{D}\right)$$





CCM flyback example: Determination of U



CCM flyback model

Express load power P_{load} in terms of V and I:

$$P_{load} = D'V\frac{I}{n}$$

Previously-derived expression for S:

$$S = V_{Q1,pk}\,I_{Q1,rms} = \left(V_g + \frac{V}{n}\right)\left(I\sqrt{D}\right)$$

Hence switch utilization U is

$$U = \frac{P_{load}}{S} = D'\sqrt{D}$$

Flyback example: switch utilization *U(D)*

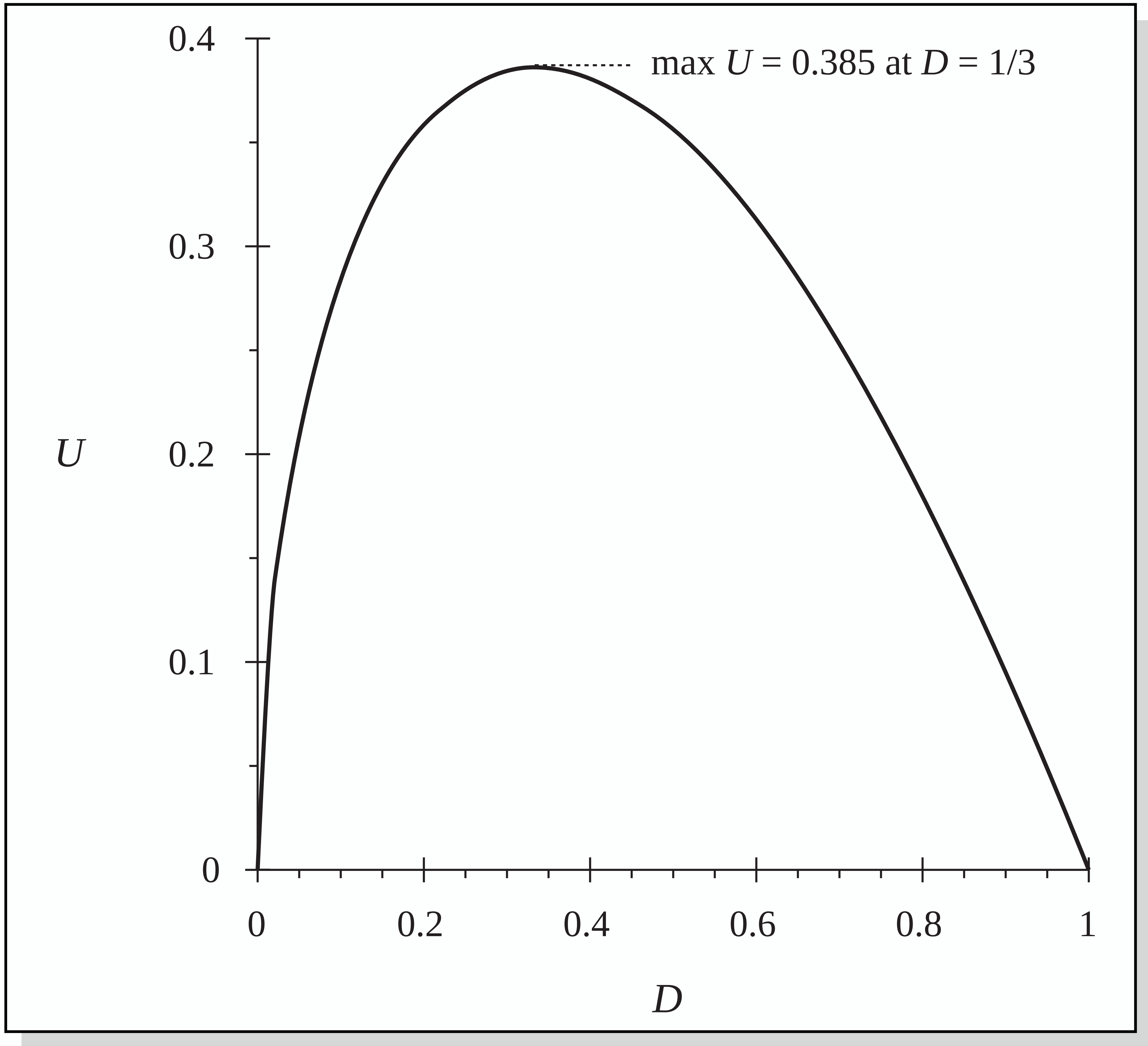
For given V, V_g, P_{load}, the designer can arbitrarily choose D. The turns ratio n must then be chosen according to

$$n = \frac{V}{V_g}\frac{D'}{D}$$

Single operating point design: choose $D = 1/3$.

small D leads to large transistor current

large D leads to large transistor voltage



Comparison of switch utilizations of some common converters

Table 6.1. Active switch utilizations of some common dc-dc converters, single operating point.

Converter	$U(D)$	max $U(D)$	max $U(D)$ *occurs at* $D =$
Buck	$\sqrt{D}$	1	1
Boost	$\frac{D'}{\sqrt{D}}$	∞	0
Buck-boost, flyback, nonisolated SEPIC, isolated SEPIC, nonisolated Cuk, isolated Cuk	$D'\sqrt{D}$	$\frac{2}{3\sqrt{3}} = 0.385$	$\frac{1}{3}$
Forward, $n_1 = n_2$	$\frac{1}{2}\sqrt{D}$	$\frac{1}{2\sqrt{2}} = 0.353$	$\frac{1}{2}$
Other isolated buck-derived converters (full-bridge, half-bridge, push-pull)	$\frac{\sqrt{D}}{2\sqrt{2}}$	$\frac{1}{2\sqrt{2}} = 0.353$	1
Isolated boost-derived converters (full bridge, push-pull)	$\frac{D'}{2\sqrt{1+D}}$	$\frac{1}{2}$	0

Switch utilization : Discussion

- Increasing the range of operating points leads to reduced switch utilization
- Buck converter
  - can operate with high switch utilization (U approaching 1) when D is close to 1
- Boost converter
  - can operate with high switch utilization (U approaching ∞) when D is close to 1
- Transformer isolation leads to reduced switch utilization
- Buck-derived transformer-isolated converters
  - $U \leq 0.353$
  - should be designed to operate with D as large as other considerations allow
  - transformer turns ratio can be chosen to optimize design

Switch utilization: Discussion

- Nonisolated and isolated versions of buck-boost, SEPIC, and Cuk converters

  $U \leq 0.385$

  Single-operating-point optimum occurs at $D = 1/3$

  Nonisolated converters have lower switch utilizations than buck or boost

  Isolation can be obtained without penalizing switch utilization

Active semiconductor cost vs. switch utilization

$$\begin{pmatrix}\text{semiconductor cost}\\ \text{per kW output power}\end{pmatrix} = \frac{\begin{pmatrix}\text{semiconductor device cost}\\ \text{per rated kVA}\end{pmatrix}}{\begin{pmatrix}\text{voltage}\\ \text{derating}\\ \text{factor}\end{pmatrix}\begin{pmatrix}\text{current}\\ \text{derating}\\ \text{factor}\end{pmatrix}\begin{pmatrix}\text{converter}\\ \text{switch}\\ \text{utilization}\end{pmatrix}}$$

(semiconductor device cost per rated kVA) = cost of device, divided by product of rated blocking voltage and rms current, in $\$/\mathrm{kVA}$. Typical values are less than $\$1/\mathrm{kVA}$

(voltage derating factor) and (current derating factor) are required to obtain reliable operation. Typical derating factors are 0.5 - 0.75

Typical cost of active semiconductor devices in an isolated dc-dc converter: \$1 - \$10 per kW of output power.

6.4.2. Converter design using computer spreadsheet

Given ranges of V_g and P_{load} , as well as desired value of V and other quantities such as switching frequency, ripple, etc., there are two basic engineering design tasks:

- Compare converter topologies and select the best for the given specifications
- Optimize the design of a given converter

A computer spreadsheet is a very useful tool for this job. The results of the steady-state converter analyses of Chapters 1-6 can be entered, and detailed design investigations can be quickly performed:

- Evaluation of worst-case stresses over a range of operating points
- Evaluation of design tradeoffs

Spreadsheet design example

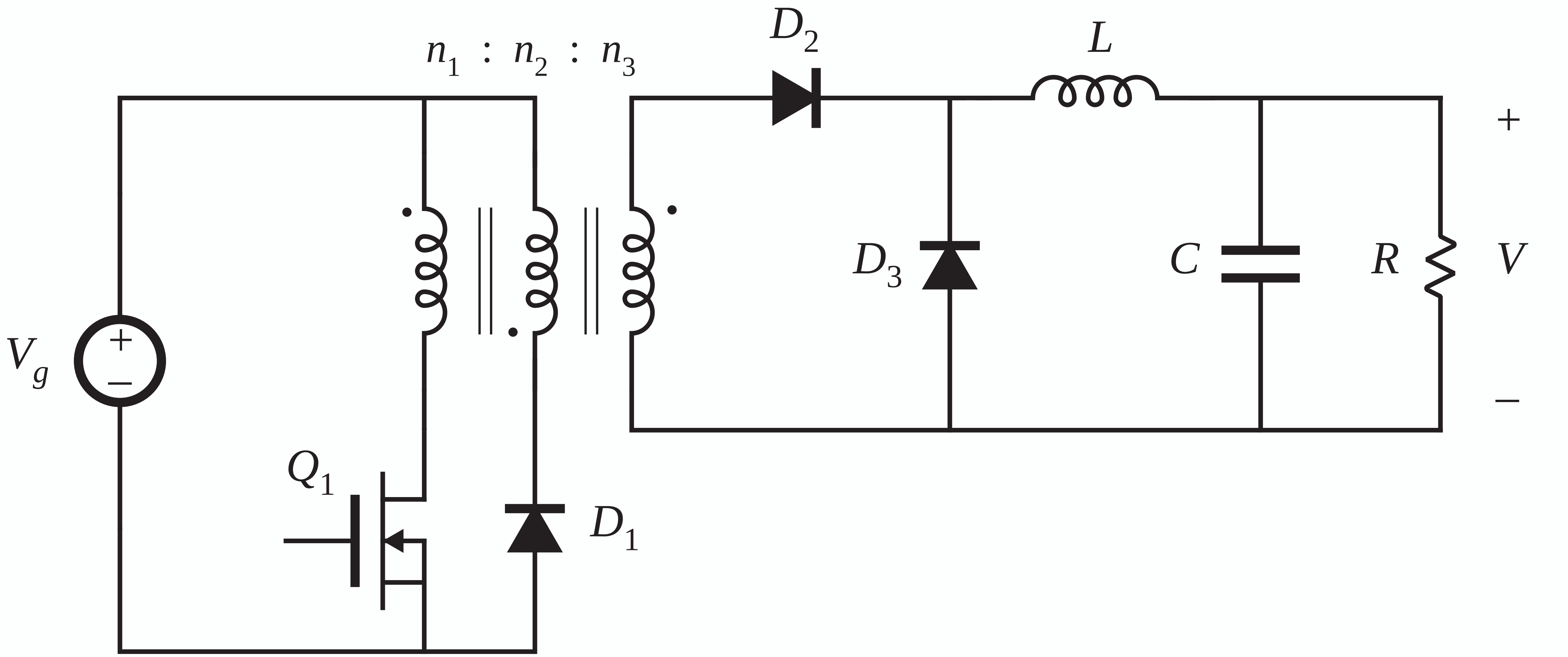
Specifications	
Maximum input voltage V_g	390 V
Minimum input voltage V_g	260 V
Output voltage V	15 V
Maximum load power P_{load}	200 W
Minimum load power P_{load}	20 W
Switching frequency f_s	100 kHz
Maximum output ripple Δv	0.1 V

- Input voltage: rectified 230 Vrms ±20%
- Regulated output of 15 V
- Rated load power 200 W
- Must operate at 10% load
- Select switching frequency of 100 kHz
- Output voltage ripple ≤ 0.1V

Compare single-transistor forward and flyback converters in this application

Specifications are entered at top of spreadsheet

Forward converter design, CCM

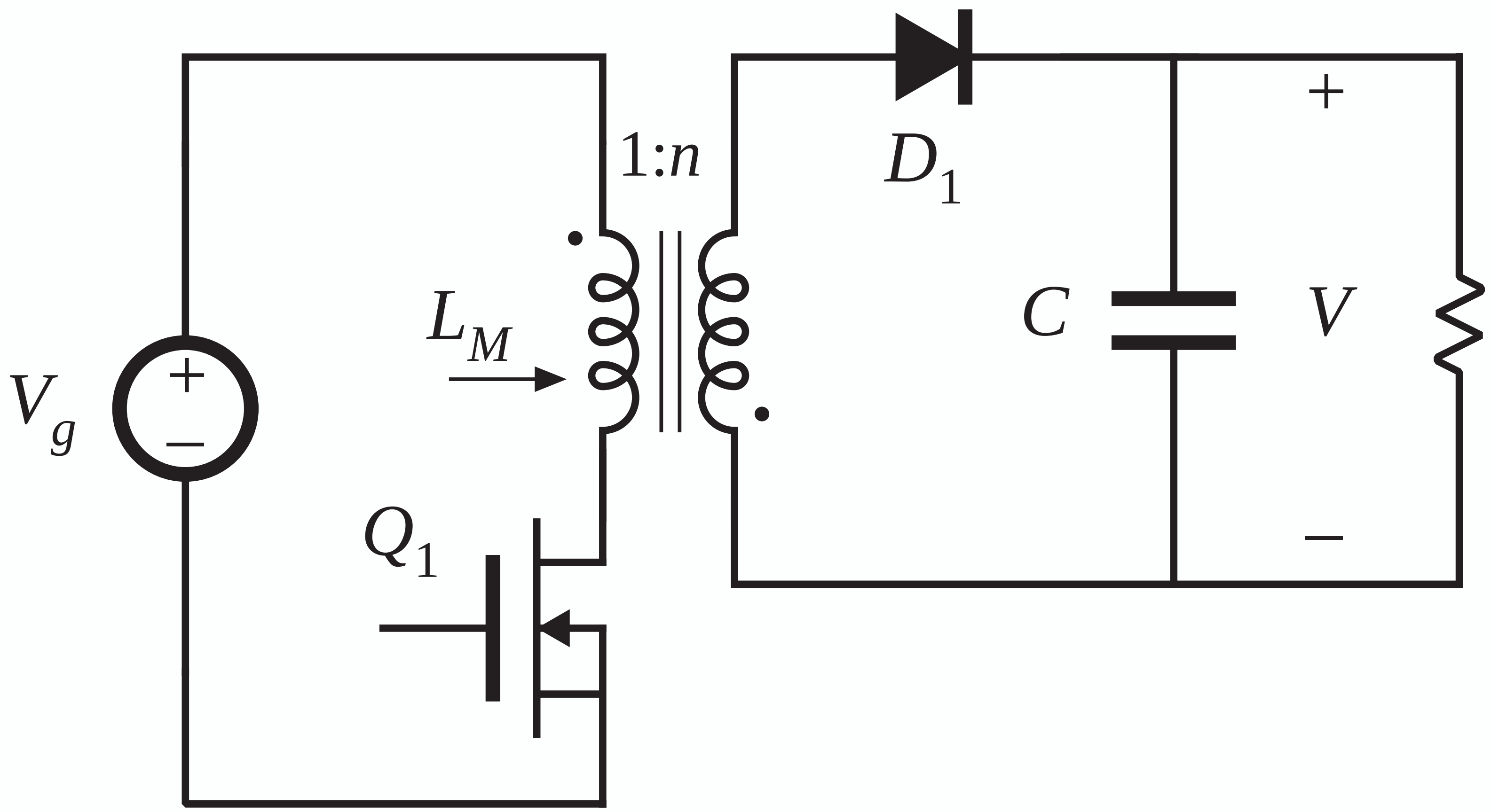


Design variables

Reset winding turns ratio n_2 / n_1	1
Turns ratio n_3 / n_1	0.125
Inductor current ripple Δi	2A ref to sec

- Design for CCM at full load; may operate in DCM at light load

Flyback converter design, CCM



Design variables

Turns ratio n_2 / n_1	0.125
Inductor current ripple Δi	3 A ref to sec

- Design for CCM at full load; may operate in DCM at light load

Enter results of converter analysis into spreadsheet (Forward converter example)

Maximum duty cycle occurs at minimum V_g and maximum P_{load}. Converter then operates in CCM, with

$$D = \frac{n_1}{n_3} \frac{V}{V_g}$$

Inductor current ripple is

$$\Delta i = \frac{D'VT_s}{2L}$$

Solve for L:

$$L = \frac{D'VT_s}{2\Delta i}$$

Δi is a design variable. For a given Δi, the equation above can be used to determine L. To ensure CCM operation at full load, Δi should be less than the full-load output current. C can be found in a similar manner.

Forward converter example, continued

Check for DCM at light load. The solution of the buck converter operating in DCM is

$$V = \frac{n_3}{n_1} V_g \frac{2}{\sqrt{1 + \frac{4K}{D^2}}}$$

with $K = 2\,L\,/\,R\,T_s$, and $R = V^2\,/\,P_{load}$

These equations apply equally well to the forward converter, provided that all quantities are referred to the transformer secondary side.

Solve for D:

$$D = \frac{2\sqrt{K}}{\sqrt{\left(\frac{2n_3V_g}{n_1V} - 1\right)^2 - 1}} \quad \text{in DCM}$$

$$D = \frac{n_1}{n_3}\frac{V}{V_g} \quad \text{in CCM}$$

at a given operating point, the actual duty cycle is the small of the values calculated by the CCM and DCM equations above. Minimum D occurs at minimum P_{load} and maximum V_g.

More regarding forward converter example

Worst-case component stresses can now be evaluated.

Peak transistor voltage is

$$\max\left(v_{Q1}\right) = V_g\left(1 + \frac{n_1}{n_2}\right)$$

RMS transistor current is

$$I_{Q1,rms} = \frac{n_3}{n_1}\sqrt{D}\sqrt{I^2 + \frac{\left(\Delta i\right)^2}{3}} \approx \frac{n_3}{n_1}\sqrt{D}\, I$$

(this neglects transformer magnetizing current)

Other component stresses can be found in a similar manner.
Magnetics design is left for a later chapter.

Results: forward and flyback converter spreadsheets

Forward converter design, CCM		*Flyback converter design, CCM*	
Design variables		*Design variables*	
Reset winding turns ratio n_2/n_1	1	Turns ratio n_2/n_1	0.125
Turns ratio n_3/n_1	0.125	Inductor current ripple Δi	3 A ref to sec
Inductor current ripple Δi	2 A ref to sec		
Results		*Results*	
Maximum duty cycle D	0.462	Maximum duty cycle D	0.316
Minimum D, at full load	0.308	Minimum D, at full load	0.235
Minimum D, at minimum load	0.251	Minimum D, at minimum load	0.179
Worst-case stresses		*Worst-case stresses*	
Peak transistor voltage v_{Q1}	780 V	Peak transistor voltage v_{Q1}	510 V
Rms transistor current i_{Q1}	1.13 A	Rms transistor current i_{Q1}	1.38 A
Transistor utilization U	0.226	Transistor utilization U	0.284
Peak diode voltage v_{D2}	49 V	Peak diode voltage v_{D1}	64 V
Rms diode current i_{D2}	9.1 A	Rms diode current i_{D1}	16.3 A
Peak diode voltage v_{D3}	49 V	Peak diode current i_{D1}	22.2 A
Rms diode current i_{D3}	11.1 A		
Rms output capacitor current i_C	1.15 A	Rms output capacitor current i_C	9.1 A

Discussion: transistor voltage

Flyback converter

Ideal peak transistor voltage: 510V

Actual peak voltage will be higher, due to ringing causes by transformer leakage inductance

An 800V or 1000V MOSFET would have an adequate design margin

Forward converter

Ideal peak transistor voltage: 780V, 53% greater than flyback

Few MOSFETs having voltage rating of over 1000 V are available—when ringing due to transformer leakage inductance is accounted for, this design will have an inadequate design margin

Fix: use two-transistor forward converter, or change reset winding turns ratio

A conclusion: reset mechanism of flyback is superior to forward

Discussion: rms transistor current

Forward

1.13A worst-case

transistor utilization 0.226

Flyback

1.38A worst case, 22% higher than forward

transistor utilization 0.284

CCM flyback exhibits higher peak and rms currents. Currents in DCM flyback are even higher

Discussion: secondary-side diode and capacitor stresses

Forward

peak diode voltage 49V

rms diode current 9.1A / 11.1A

rms capacitor current 1.15A

Flyback

peak diode voltage 64V

rms diode current 16.3A

peak diode current 22.2A

rms capacitor current 9.1A

Secondary-side currents, especially capacitor currents, limit the practical application of the flyback converter to situations where the load current is not too great.

Summary of key points

1. The boost converter can be viewed as an inverse buck converter, while the buck-boost and Cuk converters arise from cascade connections of buck and boost converters. The properties of these converters are consistent with their origins. Ac outputs can be obtained by differential connection of the load. An infinite number of converters are possible, and several are listed in this chapter.

2. For understanding the operation of most converters containing transformers, the transformer can be modeled as a magnetizing inductance in parallel with an ideal transformer. The magnetizing inductance must obey all of the usual rules for inductors, including the principle of volt-second balance.

Summary of key points

3. The steady-state behavior of transformer-isolated converters may be understood by first replacing the transformer with the magnetizing-inductance-plus-ideal-transformer equivalent circuit. The techniques developed in the previous chapters can then be applied, including use of inductor volt-second balance and capacitor charge balance to find dc currents and voltages, use of equivalent circuits to model losses and efficiency, and analysis of the discontinuous conduction mode.

4. In the full-bridge, half-bridge, and push-pull isolated versions of the buck and/or boost converters, the transformer frequency is twice the output ripple frequency. The transformer is reset while it transfers energy: the applied voltage polarity alternates on successive switching periods.

Summary of key points

5. In the conventional forward converter, the transformer is reset while the transistor is off. The transformer magnetizing inductance operates in the discontinuous conduction mode, and the maximum duty cycle is limited.
6. The flyback converter is based on the buck-boost converter. The flyback transformer is actually a two-winding inductor, which stores and transfers energy.
7. The transformer turns ratio is an extra degree-of-freedom which the designer can choose to optimize the converter design. Use of a computer spreadsheet is an effective way to determine how the choice of turns ratio affects the component voltage and current stresses.
8. Total active switch stress, and active switch utilization, are two simplified figures-of-merit which can be used to compare the various converter circuits.